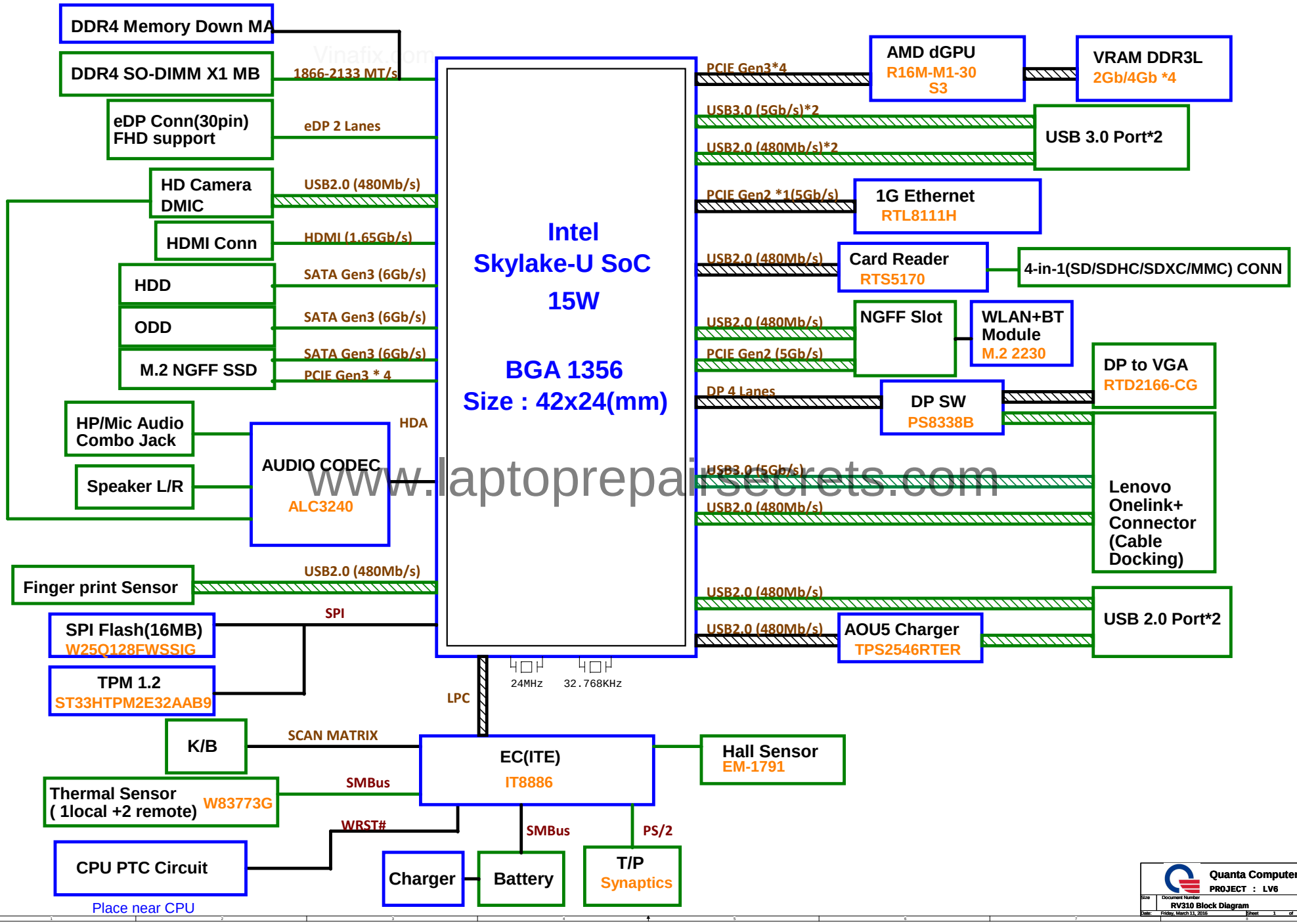
Intel Skylake-U Platform Block Diagram (Windows)



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PROJECT : LV6
RV310 Block Diagram

{4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V
{4,6,53,56} +VCCIO
{4,5,6,9,45,53,56} +VCCSTPLL

HDMI

DOCK DP

U38A — SKL_ULT — Need apply PN

DDI1_TXN[0] E55 IN_D2# {26} IN_D2#
DDI1_TXP[0] F55 IN_D2 {26} IN_D2
DDI1_TXN[1] E58 IN_D1# {26} IN_D1#
DDI1_TXP[1] F58 IN_D1 {26} IN_D1
DDI1_TXN[2] G53 IN_D0# {26} IN_D0#
DDI1_TXP[2] F56 IN_D0 {26} IN_D0
DDI1_TXN[3] G56 IN_CLK# {26} IN_CLK#
DDI1_TXP[3] IN_CLK {26} IN_CLK

DDI2_TXN[0] C50 DOCK_DDI2_TXN0 {40} DOCK_DDI2_TXN0
DDI2_TXP[0] D50 DOCK_DDI2_TXP0 {40} DOCK_DDI2_TXP0
DDI2_TXN[1] C52 DOCK_DDI2_TXN1 {40} DOCK_DDI2_TXN1
DDI2_TXP[1] D52 DOCK_DDI2_TXP1 {40} DOCK_DDI2_TXP1
DDI2_TXN[2] A50 DOCK_DDI2_TXN2 {40} DOCK_DDI2_TXN2
DDI2_TXP[2] B50 DOCK_DDI2_TXP2 {40} DOCK_DDI2_TXP2
DDI2_TXN[3] D51 DOCK_DDI2_TXN3 {40} DOCK_DDI2_TXN3
DDI2_TXP[3] C51 DOCK_DDI2_TXP3 {40} DOCK_DDI2_TXP3

DDI

GPP_E18/DDPB_CTRLCLK L13 {26} SDVO_CLK
GPP_E19/DDPB_CTRLDATA L12 {26} SDVO_DATA
GPP_E20/DDPC_CTRLCLK N7
GPP_E21/DDPC_CTRLDATA N8 +3V R203 2.2K_4
GPP_E22/DDPD_CTRLCLK N11 TP7
GPP_E23/DDPD_CTRLDATA N12
EDP_RCOMP E52 +VCCIO R175 24.9/F_4 EDP_RCOMP

DISPLAY SIDEBANDS

SKL_ULT
REV = 1
1 OF 20

EDP

EDP_TXN[0] C47 INT_EDP_TXN0 INT_EDP_TXN0 {25}
EDP_TXP[0] C46 INT_EDP_TXP0 INT_EDP_TXP0 {25}
EDP_TXN[1] D46 INT_EDP_TXN1 INT_EDP_TXN1 {25}
EDP_TXP[1] C45 INT_EDP_TXP1 INT_EDP_TXP1 {25}
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 INT_EDP_AUXN INT_EDP_AUXN {25}
EDP_AUXP F45 INT_EDP_AUXP INT_EDP_AUXP {25}

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP C50
DDI2_AUXN E48 DOCK_DDI2_AUXN DOCK_DDI2_AUXN {40}
DDI2_AUXP F48 DOCK_DDI2_AUXP DOCK_DDI2_AUXP {40}
DDI3_AUXN G46
DDI3_AUXP F46

GPP_E13/DDPB_HPD0 L9 PCH_HDMI_HPD PCH_HDMI_HPD {26}
GPP_E14/DDPC_HPD1 L7 PCH_DOCK_DP_HPD PCH_DOCK_DP_HPD {40}
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 L9
GPP_E17/EDP_HPD L10 EDP_HPD EDP_HPD {25}

EDP_BKLTEN R12 PCH_LVDS_BLON PCH_LVDS_BLON {25}
EDP_BKLTCTL R11 PCH_DPST_PWM PCH_DPST_PWM {25}
EDP_VDDEN U13 PCH_LCDVCC_EN PCH_LCDVCC_EN {25}

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V R200 10K_4 EDP_HPD R199 100K_4

+VCCSTPLL H_PROCHOT# R590 1K_4

+VCCSTPLL PM_THRMTRIP#_R R583 1K_4

B2A

U38D — SKL_ULT — Need apply PN

{36,42,43,45} H_PROCHOT# H_PROCHOT# R596 499/F_4
{36} PM_THRMTRIP# R762 100/F_4
B2A

+VCCIO R601 *51_4 {36} EC_PECI

CATERR# D63 CATERR#
PECI A54 EC_PECI
PROCHOT# C65 PROCHOT#
THERMTRIP# C63 PM_THRMTRIP#_R
SKTOCC# A65

CPU MISC

TP34 C55 BPM#[0]
TP36 D55 BPM#[1]
B54 BPM#[2]
C66 BPM#[3]

GPP_E3/CPU_GP0 A6
GPP_E7/CPU_GP1 A7
GPP_B3/CPU_GP2 BA5
GPP_B4/CPU_GP3 AY5
TP49

PROC_POPIRCOMP AT16 R278 49.9/F_4 PROC_POPIRCOMP
PCH_OPIRCOMP AU16 R277 49.9/F_4 PCH_OPI_RCOMP
OPCE_RCOMP H66 R620 GT3@49.9/F_4 EDRAM_OPIO_RCOMP
OPC_RCOMP H65 R626 GT3@49.9/F_4 EOPIO_RCOMP

JTAG

PROC_TCK B61 XDP_TCK0
PROC_TDI A61 XDP_TDO
PROC_TDO G60 XDP_TMS
PROC_TMS B59 XDP_TRST#
PROC_TRST# TP35

PCH_JTAG_TCK B56 XDP_TCK1
PCH_JTAG_TDI D59 XDP_TDI
PCH_JTAG_TDO A56 XDP_TDO
PCH_JTAG_TMS C59 XDP_TMS
PCH_TRST# C61 XDP_TRST#
JTAGX A59 XDP_TCK0

SKL_ULT
REV = 1
4 OF 20

+VCCIO

XDP_TMS R576 *51_4
XDP_TDO R588 51_4
XDP_TDI R581 *51_4
XDP_TCK0 R602 51_4
XDP_TCK1 R603 *51_4
EC_PECI R792 KBY@330_4

PLACE NEAR CPU

D3A

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Size	Document Number	Rev
	SKYLAKE 1/15 eDP/DDI/MISC	1A

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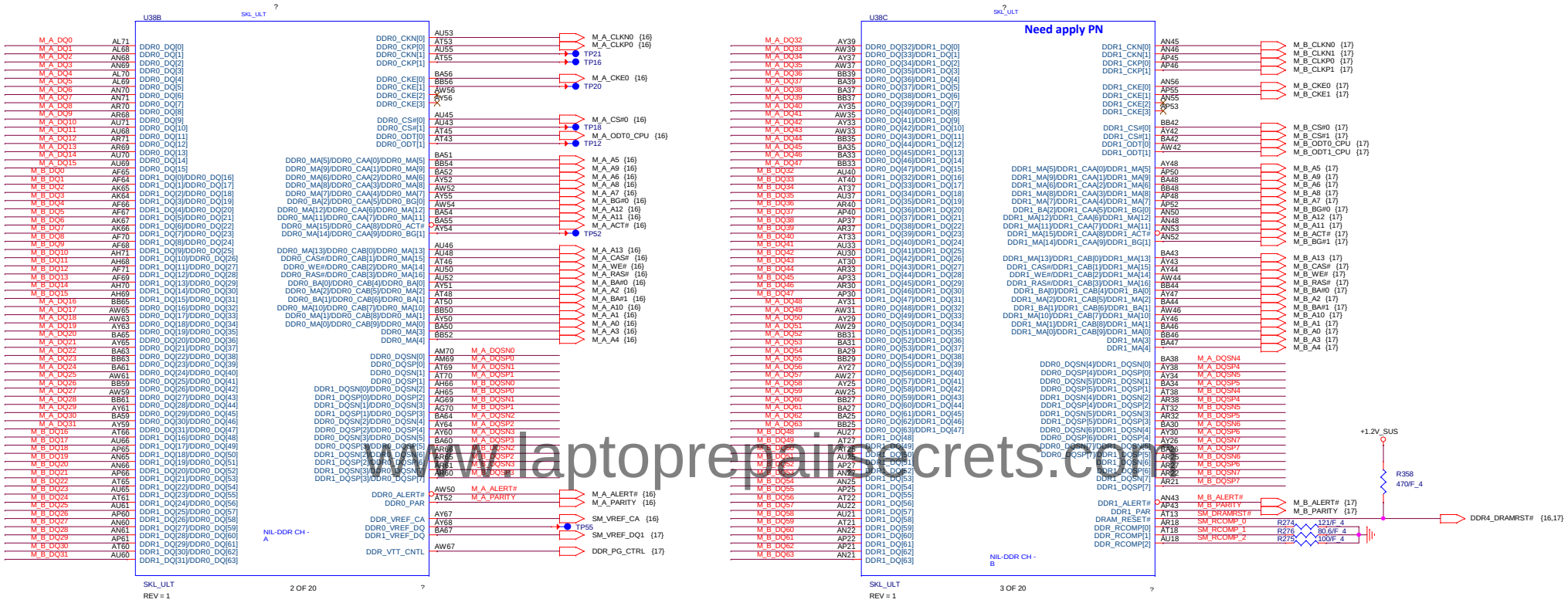
SkyLake ULT Processor (DDR4) Interleave

03



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Quanta Computer Inc.	
PROJECT : LV6	
Size	Document Number: SKYLAKE 2/15(DDR4 I/F) — Rev: 1A
Date: Friday, March 11, 2016	Sheet 3 of 61

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{10,11,14,15,17} +3V_DEEP_SUS
{10,12,15,26,28,30,32,33,35,36,41,42,44,49,51,53,54,56} +3VS5
{2,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V
{34,35,38,39,41,42,44,45,48,50,51,53,54,56} +5VS5
{2,6,53,56} +VCCIO
{2,5,6,9,45,53,56} +VCCSTPLL
{13,15} +3V_RTC_2

U38K SKL_ULT ?
SYSTEM POWER MANAGEMENT

{36} RSMRST# PLTRST# SYS_RESET# RSMRST# AN10 B5 AY17
R595 10K_4 PROCPWRGD H_VCCST_PWRGD A68 B65
{29,36,37} EC_PWROK C276 *0.1U/16V/X7R_4 SYS_PWROK EC_PWROK DSWROK_EC_R B6 BA20 BB20
SUSWARN# SUSACK# AR13 AP11
*0_4_S R295
{19,30,33} PCIE_WAKE# PCIE_WAKE# GPD2 BB15 AM15
B2A TP50 TP15 AW17 AT15

GPP_B13/PLTRST# SYS_RESET# RSMRST#
PROCPWRGD VCCST_PWRGD
SYS_PWROK PCH_PWROK DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK GPP_A15/SUSACK#
WAKE# GPD2/LAN_WAKE# GPD11/LANPHYPC GPD7/RSVD

SKL_ULT REV = 1
11 OF 20
?

GPP_B12/SLP_S0# AT11 PCH_SLP_S0# PCH_SLP_S0# {36}
GPD4/SLP_S3# AP15 SUSB# {18,36}
GPD5/SLP_S4# BA16 SUSC# {36}
GPD10/SLP_S5# AY16 SLP_S5# TP53
SLP_SUS# AN15
SLP_LAN# AW15 SLP_LAN# TP51
GPD9/SLP_WLAN# BB17 TP13 SLP_WLAN# {33}
GPD6/SLP_A# AN16
GPD3/PWRBTN# BA15 DNBSWON# DNBSWON# {36}
GPD1/ACPRESENT AY15 AC_PRESENT_EC AC_PRESENT_EC {36}
GPD0/BATLOW# AU13 PM_BATLOW_N_EC PM_BATLOW_N_EC {36}
GPP_A11/PME# AU11
INTRUDER# AP16 INTRUDER#_R R287 1M_4 +3V_RTC_2
GPP_B11/EXT_PWR_GATE# AM10 EXT_PWR_GATE#
GPP_B2/VRALERT# AM11 PCH_VRALERT#
B2A

C3A

PCH Pull-high/low(CLG)

+3V_DEEP_SUS
SUSWARN# R297 10K_4
SUSACK# R293 *10K_4
PM_BATLOW_N_EC R302 10K_4
GPD2 R763 10K_4
B2A

+3VS5
PCIE_WAKE# R687 10K_4
AC_PRESENT_EC R692 10K_4
DNBSWON# R780 *10K_4
C3A
+3V
SYS_RESET# R196 10K_4
PCH_VRALERT# R764 10K_4
B2A

RSMRST# R688 10K_4
DSWROK_EC_R R288 100K_4
EXT_PWR_GATE# R251 1K_4 +3VS5

RSMRST#
SYS_RESET#
PLTRST#
EC13 *E@220P/50V_4
EC9 *E@220P/50V_4
EC38 *E@220P/50V_4

RSMRST# R285 *0_4_S DSWROK_EC_R

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PLTRST#(CLG)

{18,28,30,31,33,36,37} PLTRST# PLTRST# R437 100K_4

+VCCIO +VCCSTPLL
R591 1K_4
R582 *1K_4
{36,49,50} HWPG HWPG D17 1 2 DB2J40600L H_VCCST_PWRGD_R R597 60.4_4 H_VCCST_PWRGD
C688 *10P/50V_4

+VCCIO +5VS5 +3VS5
R569 15K_4
R559 100K_4
R558 10K_4
HWPG
+1.0V_PWRGD_G2 2 Q39 2N7002K
R557 100K_4
+1.0V_PWRGD_G1 2 Q38 METR3904-G
C665 0.1U/16V/X7R_4
R565 100K_4

System PWR_OK(CLG)

{36} SYS_PWROK SYS_PWROK R190 *0_4 EC_PWROK
R189 100K_4
R192 100K_4

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PROJECT : LV6
Size | Document Number: SKYLAKE 3/15(PowerManger) | Rev: 1A
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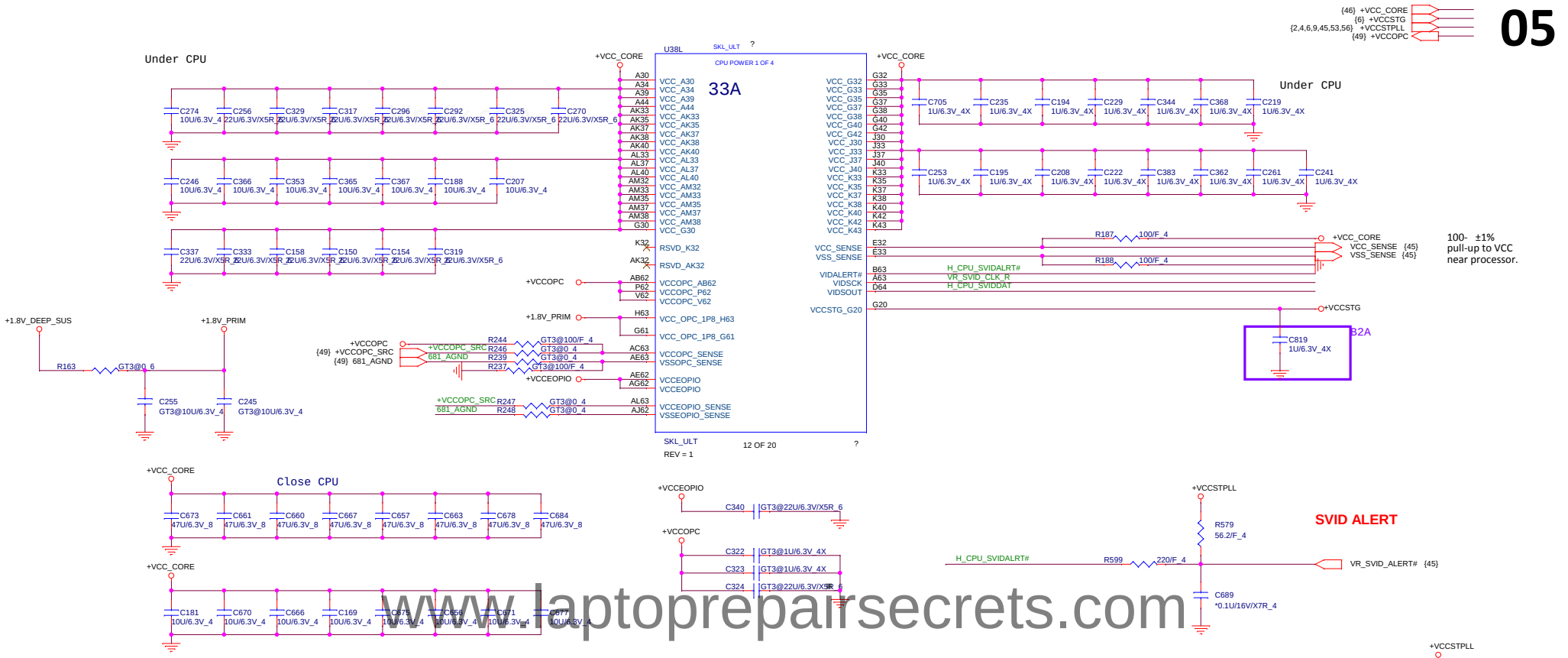

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Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Quanta Computer Inc.
PROJECT : LV6
Size | Document Number: SKYLAKE 4/15 (POWER-1) | Rev 1A
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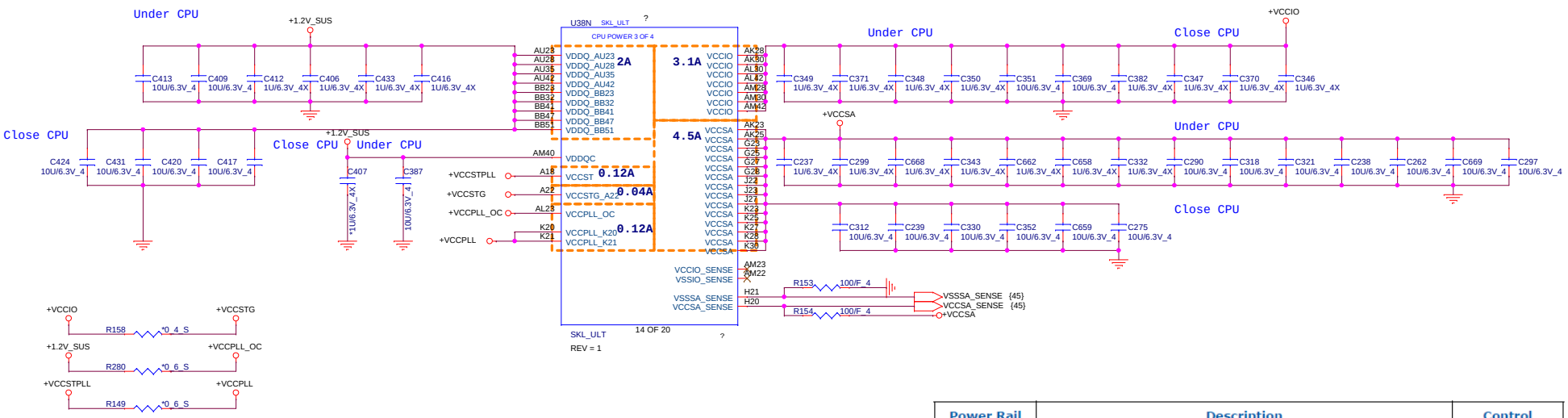

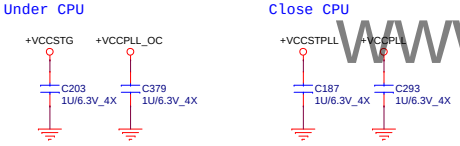

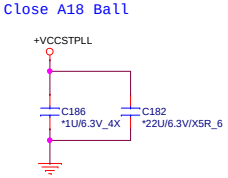

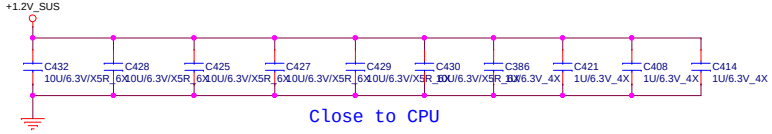

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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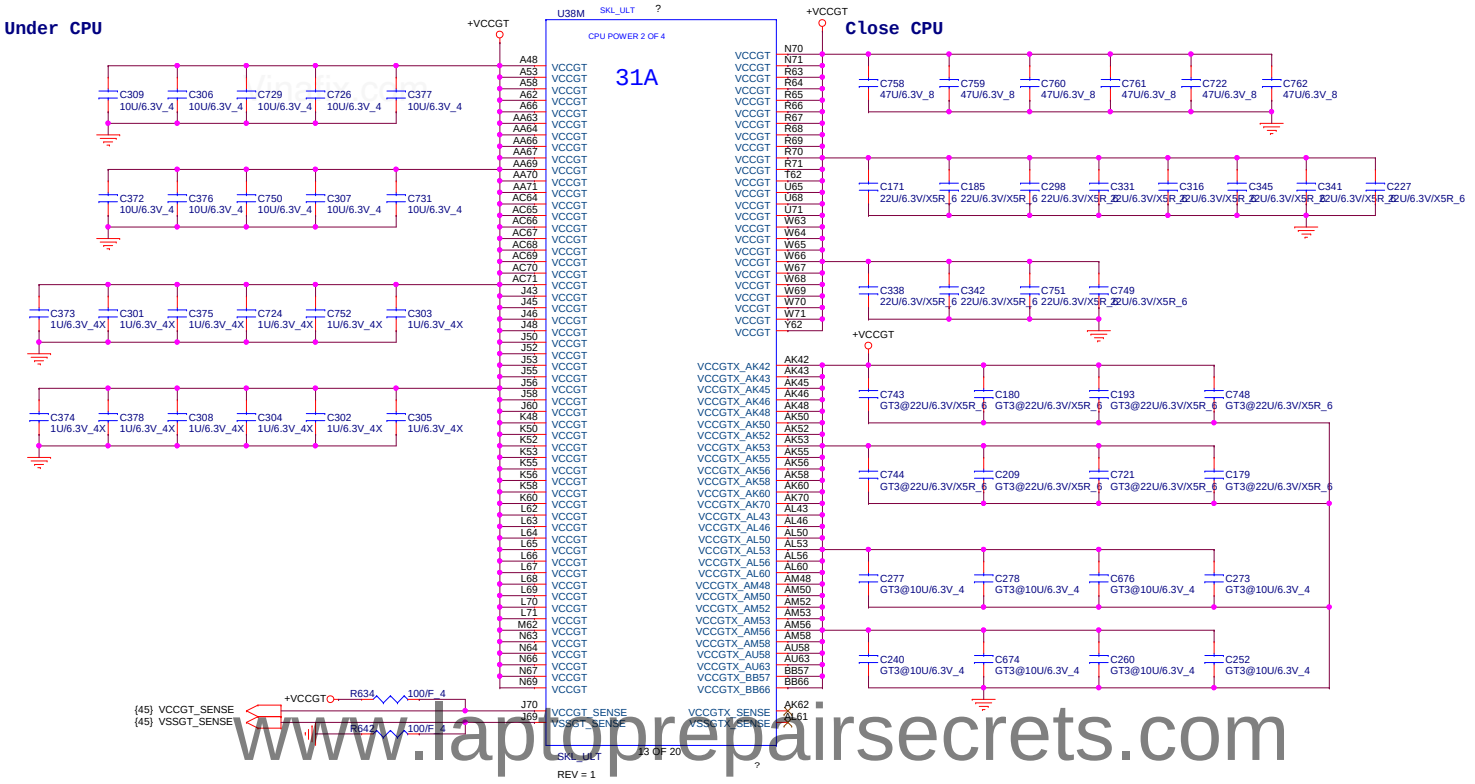

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Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Size | Document Number: SKYLAKE 6/15 (POWER-3) | Rev 1A
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PROJECT : LV6		
Size	Document Number	Rev
	SKYLAKE 7/15 (GND)	1A
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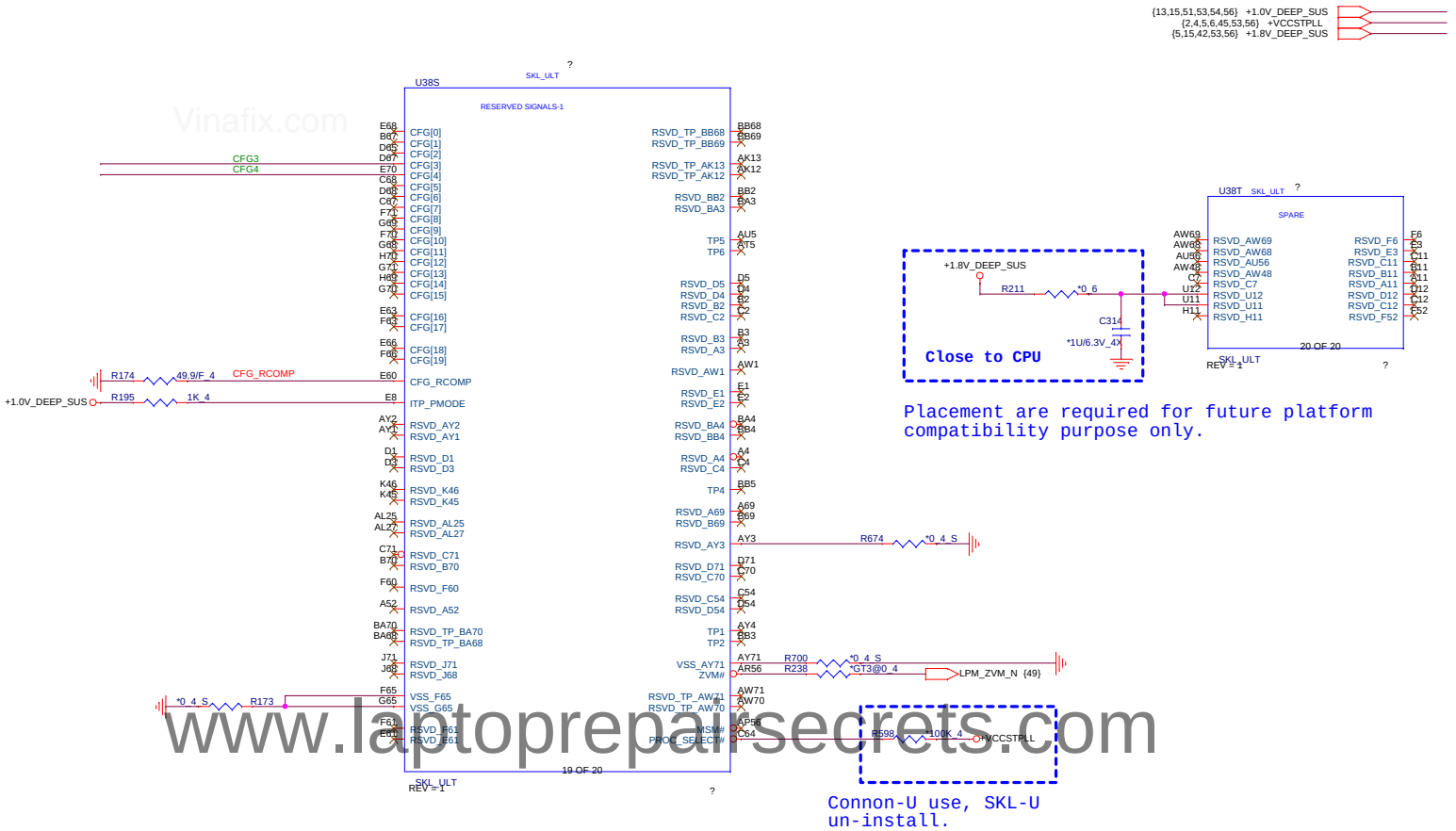

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Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R611 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R617 1K_4

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PROJECT : LV6

Size	Document Number	Rev
	SKYLAKE 8/15 (RSV)	1A

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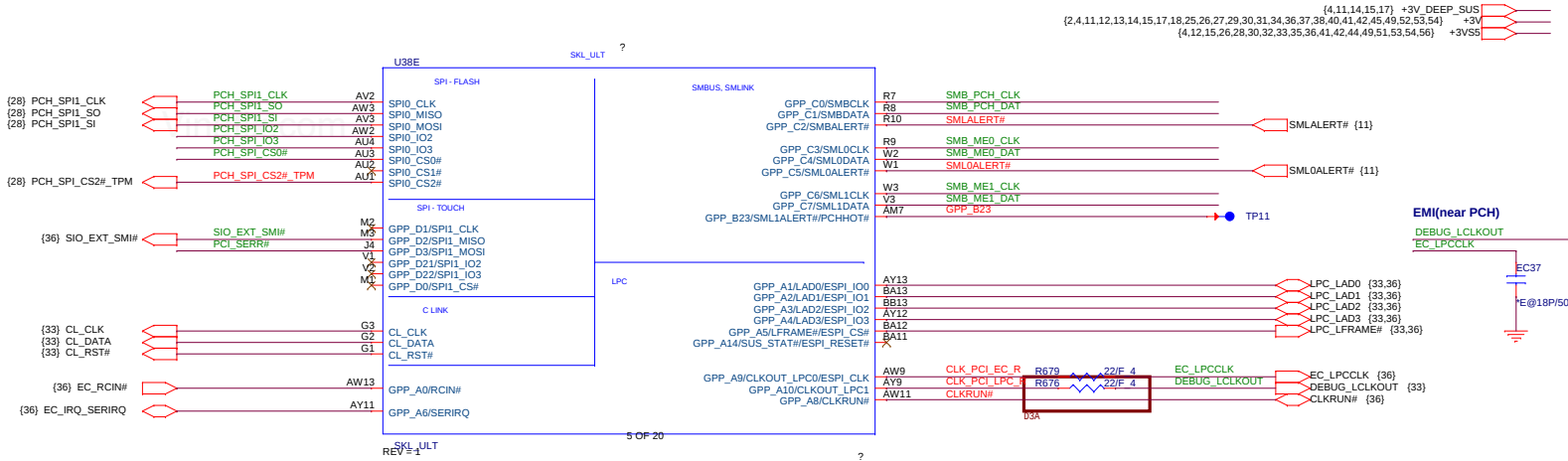
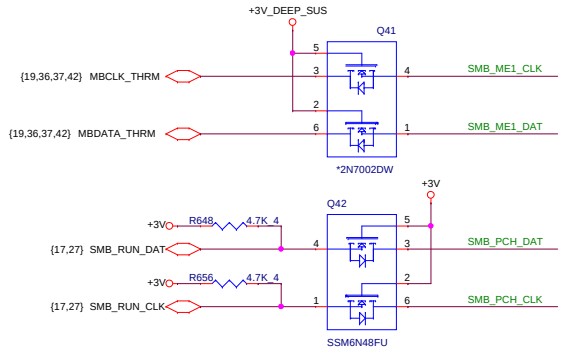
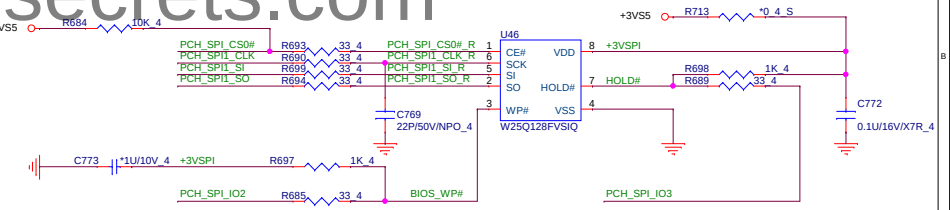


GPIO Pull UP

SMBus/Pull-up(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	16MB	AKE3DZNKQ00(EN25QH128AHIP)
GGD	16MB	AKE3DF00Q00 (GD25B128CSIGR)
Socket		DFHS08FS023

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Size | Document Number: SKYLAKE 9/15(SPI/LPC/SM) | Rev: 1A
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Functional Strap Definitions

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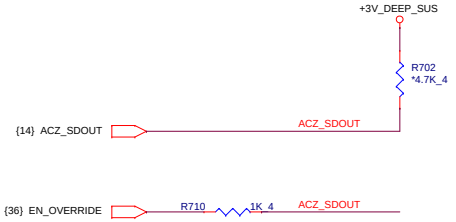
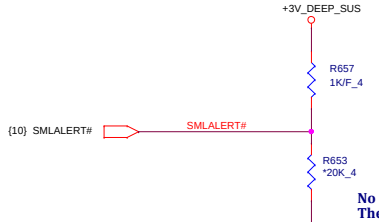
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

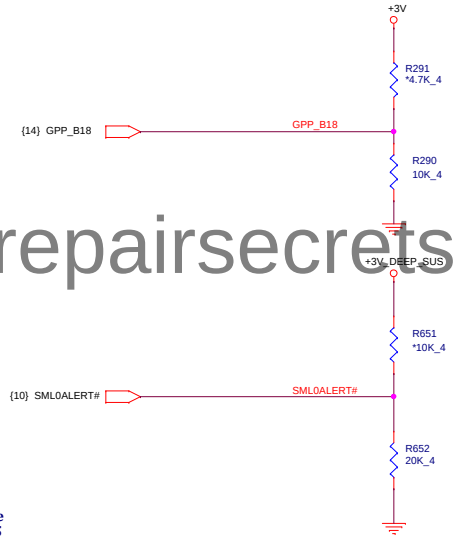
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



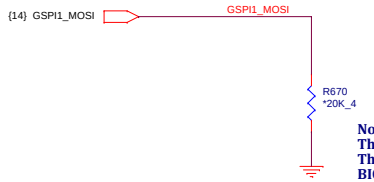
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system Reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC

No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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PROJECT : LV6

Size	Document Number	Rev
	SKYLAKE 10/15(Strip)	1A
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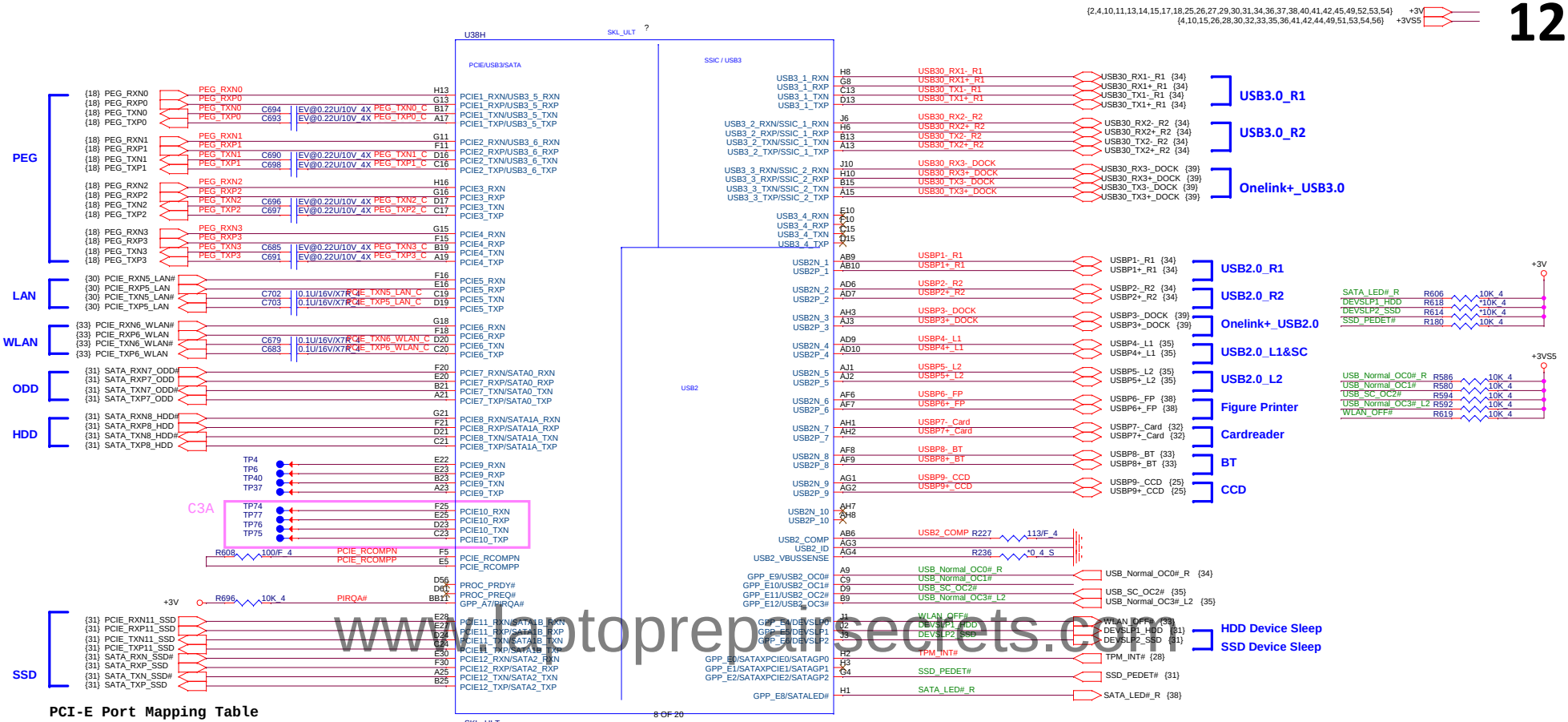

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PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	dGPU
Port2		Port1	LAN
Port3		Port2	WLAN
Port4		Port3	DOCK
Port5	LAN	Port4	Un-used
Port6	WLAN	Port5	SSD
Port7	ODD		
Port8	HDD		
Port9	Un-used		
Port10	DOCK		
Port11	SSD if Pcie Bus will lane reverse. if SATA BUS is SATA2.		
Port12			

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0_R1
PORT-2	USB3.0_R2
PORT-3	USB3.0_DOCK
PORT-4	

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB2.0_R1
PORT-2	USB2.0_R2
PORT-3	USB2.0_DOCK
PORT-4	USB2.0_L1_S&C
PORT-5	USB2.0_L2
PORT-6	Figure Printer
PORT-7	Cardreader
PORT-8	BT
PORT-9	CCD
PORT-10	NC

Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	SKYLAKE 11/15 (PCIE/USB)	1A

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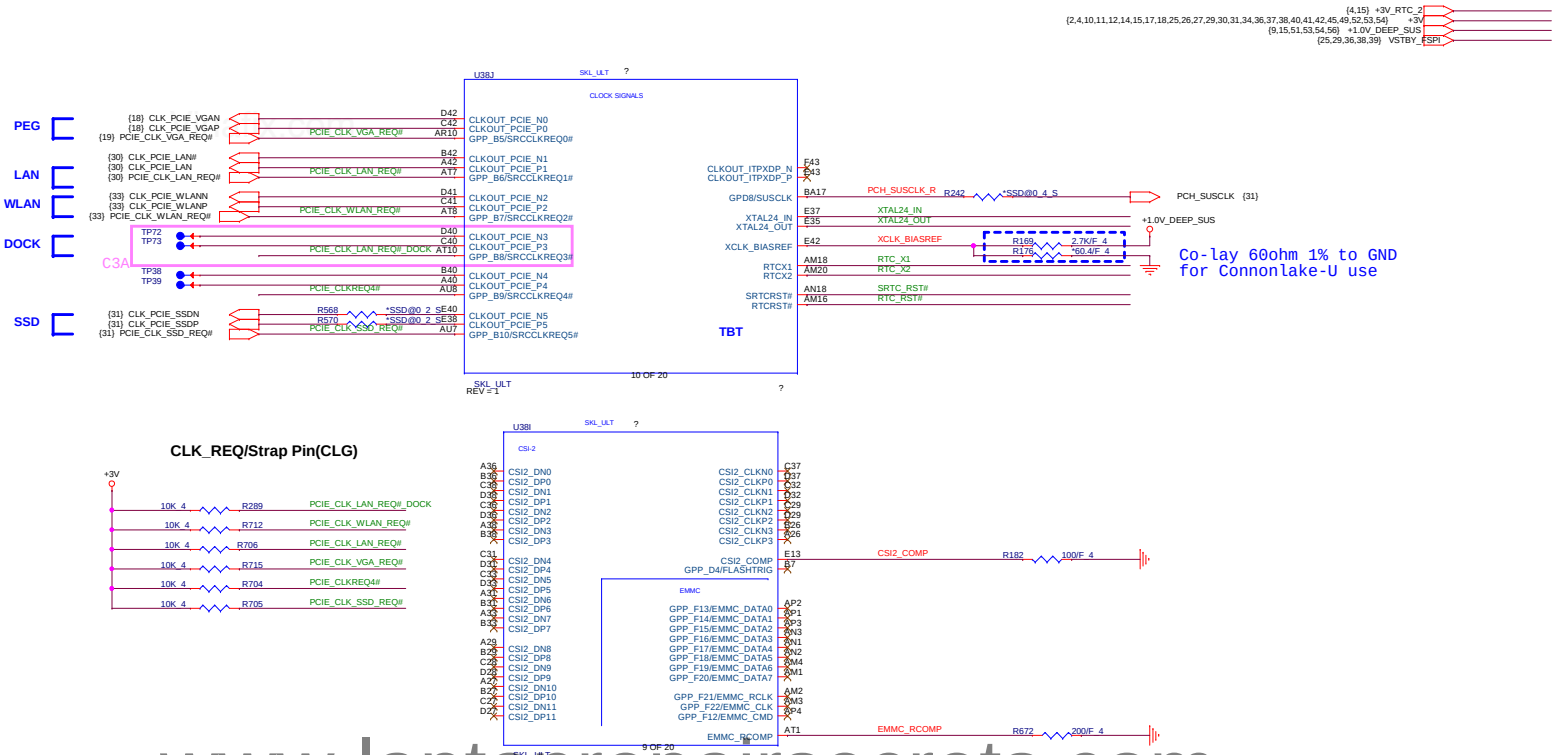

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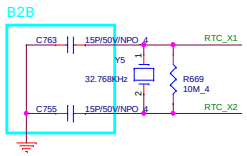
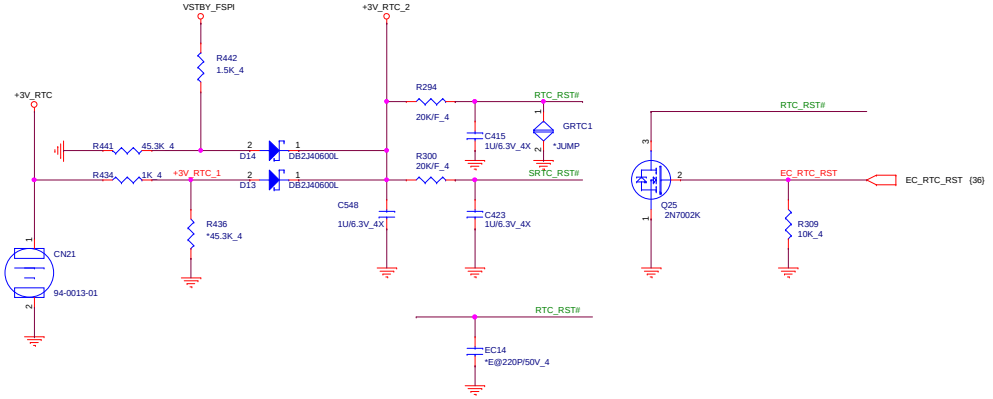
RTC Clock 32.768KHz (RTC)<RTC>

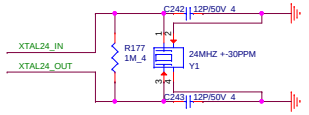


RTC Circuitry (RTC) <RTC>

RTC Power trace width 20mils.



External Crystal and Green Clock

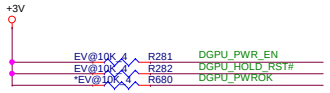


Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	SKYLAKE 12/15 (CLK/EMMC)	1A

Date: Friday, March 11, 2016 Sheet 13 of 61

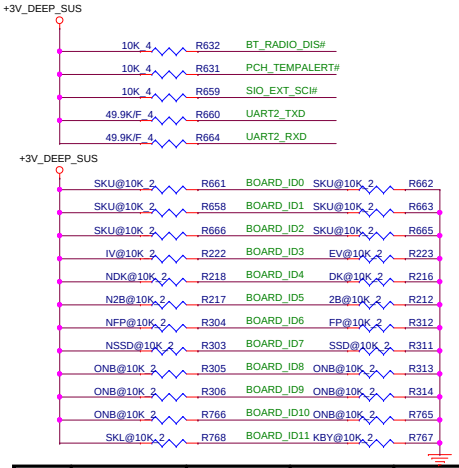
DGPU <VGA>



<CPU>

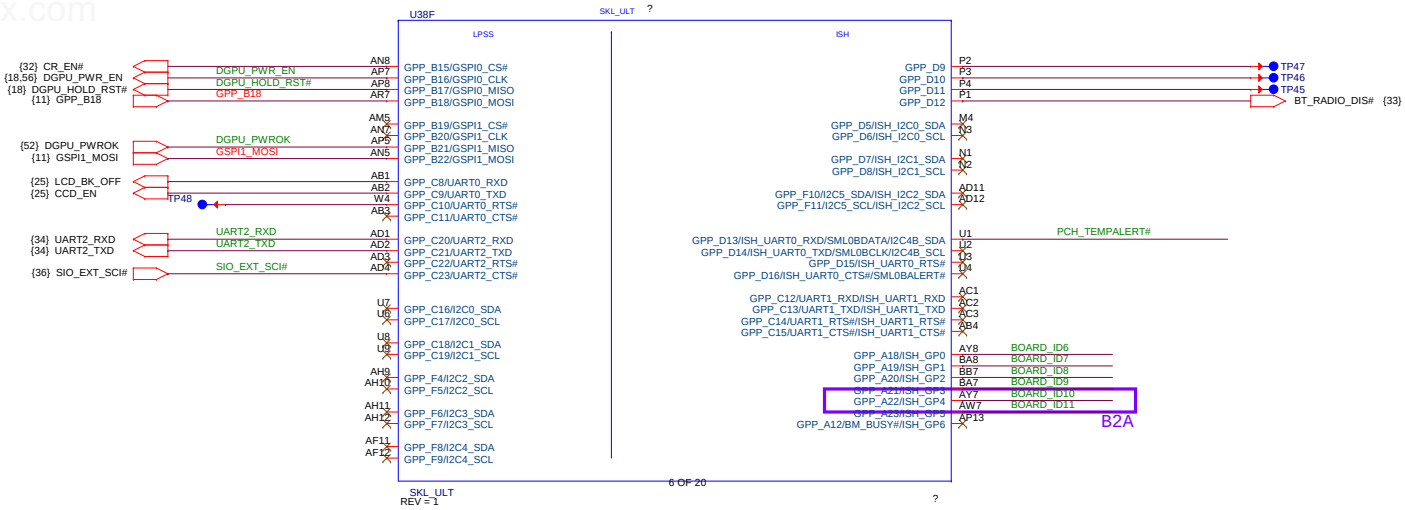
{4,10,11,15,17} +3V_DEEP_SUS
{2,4,10,11,12,13,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V

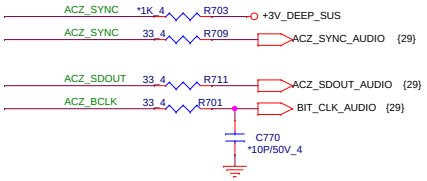
Skylake (GPIO)



Sku	Model	BOARD_ID0	BOARD_ID1	BOARD_ID2
0	E42(R310_14)	0	0	0
1	E52(R310_15)	0	0	1
2	V310_14	0	1	0
3	V310_15	0	1	1
4	Tianyi310_14	1	0	0
5	Tianyi310_15	1	0	1
6	Reserved	1	1	0
7	Reserved	1	1	1

BOARD_ID3	Hi = UMA	Lo = Discrete
BOARD_ID4	Hi = wo Prolink	Lo = w Prolink
BOARD_ID5	Hi = wo 2nd Battery	Lo = w 2nd Battery
BOARD_ID6	Hi = wo Figure Printer	Lo = w Figure Printer
BOARD_ID7	Hi = wo SSD	Lo = w SSD
On Board Memory	[1, 1, 1] = Samsung K4A8G165WB-BCRC [1, 1, 0] = Micro MT40A512M16JY-083E:B [1, 0, 1] = SMART [1, 0, 0] = Teikon [0, 1, 1] = Samsung K4A8G165WB-BCPB [0, 1, 0] = Micro MT40A512M16HA-083E:A [0, 0, 1] = Hynix H5AN8G6NAFR-TFC [0, 0, 0] = No Memory Down	D3A B2A C3A B2A
BOARD_ID10		
BOARD_ID9		
BOARD_ID8		
BOARD_ID11	Hi = Skylake	Lo = Kaby lake





Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	SKYLAKE 13/15 (HDA/GPIO)	1A

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{4,10,11,14,17} +3V_DEEP_SUS
{9,13,51,53,54,56} +1.0V_DEEP_SUS
{5,9,42,53,56} +1.8V_DEEP_SUS
{4,10,12,26,28,30,32,33,35,36,41,42,44,49,51,53,54,56} +3VS5
{4,13} +3V_RTC_2
{2,4,10,11,12,13,14,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V

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U38O SKL_ULT
CPU POWER 4 OF 4
15 OF 20
SKL_ULT REV_1

+VCCPRIM
C334 1U/6.3V_4X
AB19 VCCPRIM_1P0
AB20 VCCPRIM_1P0
P18 VCCPRIM_1P0
2.899A

+1.0V_DEEP_SUS
C326 *1U/6.3V_4X
AF18 VCCPRIM_CORE
AF19 VCCPRIM_CORE
V20 VCCPRIM_CORE
V21 VCCPRIM_CORE
2.57A

+VCCDSW_1.0V
C754 1U/6.3V_4X
AL1 DCPDSW_1P0

+1.0V_DEEP_SUS
R627 *0_6_S
+VCCMPHYAON_1P0
C269 1U/6.3V_4X
K17 VCCMPHYAON_1P0
L1 VCCMPHYAON_1P0

+1.0V_DEEP_SUS
C202 1U/6.3V_4X
C177 47U/6.3V_8
N15 VCCMPHYGT_1P0_N15
N16 VCCMPHYGT_1P0_N16
N17 VCCMPHYGT_1P0_N17
P15 VCCMPHYGT_1P0_P15
P16 VCCMPHYGT_1P0_P16
1.714A

+1.0V_DEEP_SUS
R202 *0_4_S
+VCCAMPHYPLL_1P0
C285 *1U/6.3V_4X
K15 VCCAMPHYPLL_1P0
L15 VCCAMPHYPLL_1P0

+1.0V_DEEP_SUS
L12 HCB1608KF-221T20_2A
+VCCAPLL_1.0V
C289 0.1U/16V/X7R_4
V15 VCCAPLL_1P0
0.03A

+1.0V_DEEP_SUS
R221 *0_6_S
R215 *0_6_S
+VCCPRIM
AB17 VCCPRIM_1P0_AB17
Y18 VCCPRIM_1P0_Y18

+3VS5
R226 *0_4_S
C354 *1U/6.3V_4X
C389 0.1U/16V/X7R_4
C388 *0.1P/50V_4
AD17 VCCDSW_3P3_AD17
AD18 VCCDSW_3P3_AD18
AJ17 VCCDSW_3P3_AJ17
0.09A

+V3.3DX_1.5DX_ADO
+V3.3DX_1.5DX_ADO_R
AJ19 VCCHDA

+3V_DEEP_SUS
R260 *0_6_S
+VCCSPI
AJ16 VCCSPI

+1.0V_DEEP_SUS
R232 *0_6_S
+VCCSRAM_1.0V
C315 *1U/6.3V_4X
AF20 VCCSRAM_1P0
AF21 VCCSRAM_1P0
T19 VCCSRAM_1P0
T20 VCCSRAM_1P0

+3V_DEEP_SUS
R258 *0_6_S
+VCCPRIM_3.3V
AJ21 VCCPRIM_3P3_AJ21

+1.0V_DEEP_SUS
R682 *0_6_S
+VCCPRIM_1.0V
AK20 VCCPRIM_1P0_AK20

+1.0V_DEEP_SUS
R198 *0_6_S
+VCCAPLLEBB
N18 VCCAPLLEBB
1U/6.3V_4X C279

VCCPGPPA AK15 +VCCPGPPA
VCCPGPPB AG15 +VCCPGPPB
VCCPGPPC Y16 +VCCPGPPC
VCCPGPPD Y15 +VCCPGPPD
VCCPGPPE T16 +VCCPGPPE
VCCPGPPF AF16 +VCCPGPPF
VCCPGPPG AD15 +VCCPGPPG

VCCPRIM_3P3_V19 V19
C404 *1U/6.3V_4X
+3V_DEEP_SUS

VCCPRIM_1P0_T1 T1
+VCCPRIM_1.0V_T1
R633 *0_6_S
+1.0V_DEEP_SUS

VCCATS_1P8 AA1
+VCCATS_1.8V
R655 *0_6_S
+1.8V_DEEP_SUS

VCCRTCPRIM_3P3 AK17
+VCCRTCPRIM_3.3V
R259 *0_6_S
+3V_DEEP_SUS

VCCRTC_AK19 AK19
VCCRTC_BB14 BB14
+VCCRTC
R286 *0_4_S
+3V_RTC_2

DCPRTC BB10
DCPRTC
C768 0.1U/16V/X7R_4

VCCCLK1 A14
+VCCCLK1
R150 *0_6_S
+1.0V_DEEP_SUS

VCCCLK2 K19
+VCCCLK2
R161 *0_4_S

VCCCLK3 L21
+VCCCLK3
R673 *0_6_S

VCCCLK4 N20
+VCCCLK4
R201 *0_4_S

VCCCLK5 L19
+VCCCLK5
R167 *0_4_S

VCCCLK6 A10
+VCCCLK6
R157 *0_6_S
C196 *1U/6.3V_4X

GPP_B0/CORE_VID0 AN11
GPP_B1/CORE_VID1 AN13
CORE_VID0
CORE_VID1
TP14
TP10

+3V_DEEP_SUS
+VCCPGPPA R234 *0_4_S
+VCCPGPPB R266 *0_4_S
+VCCPGPPC R671 *0_4_S
+VCCPGPPD R207 *0_4_S
+VCCPGPPE R205 *0_4_S
+VCCPGPPG R229 *0_4_S

+1.8V_DEEP_SUS
+VCCPGPPF R681 *0_4_S

+VCCCLK2 C220 *10U/6.3V_4
+VCCCLK4 C295 *10U/6.3V_4
+VCCCLK5 C247 *10U/6.3V_4
+VCCAMPHYPLL_1P0 C286 *10U/6.3V_4

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+V3.3DX_1.5DX_ADO L13 HCB1608KF-221T20_2A +3V

+1.0V_DEEP_SUS C213 *1U/6.3V_4X C190 *22U/6.3V/X5R_6

+3VS5 R194 *0_6_S R230 *0_6_S +3V_DEEP_SUS

+VCCATS_1.8V C745 1U/6.3V_4X
+VCCRTC C405 0.1U/16V/X7R_4 C411 1U/6.3V_4X
+VCCRTCPRIM_3.3V C396 1U/6.3V_4X C395 0.1U/16V/X7R_4

+VCCPGPPB C398 *1U/6.3V_4X
+VCCPGPPC C756 *1U/6.3V_4X
+VCCPGPPE C291 1U/6.3V_4X

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PROJECT : LV6
Size
Document Number
SKYPAKE 14/15(PCH POWER)
Rev 1A
Date: Friday, March 11, 2016
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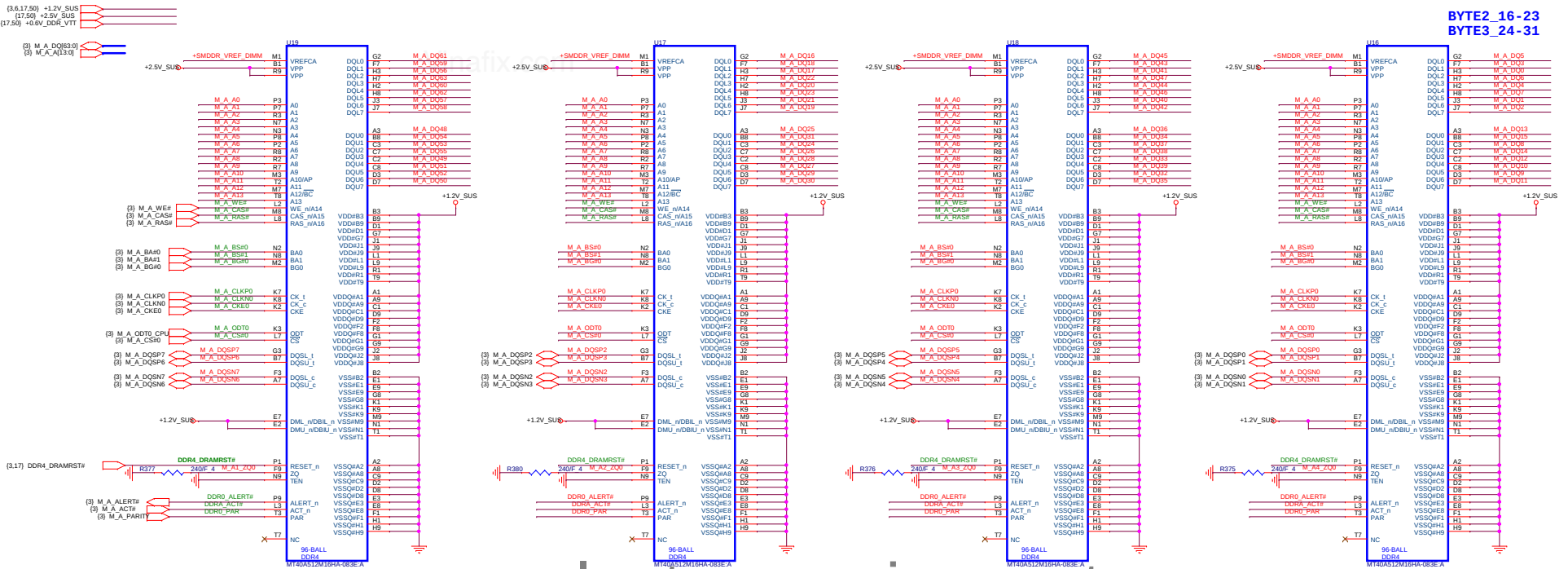
<DDR> (Memory Down)

BYTE2_16-23
BYTE3_24-31



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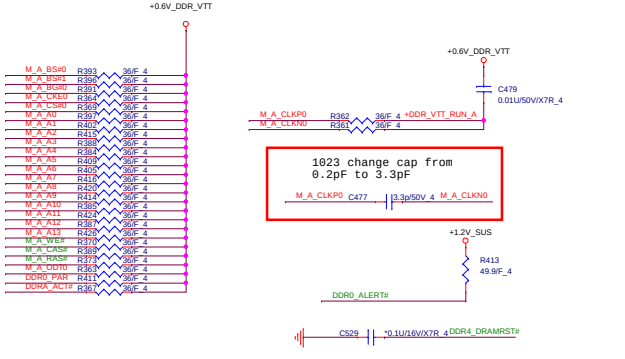
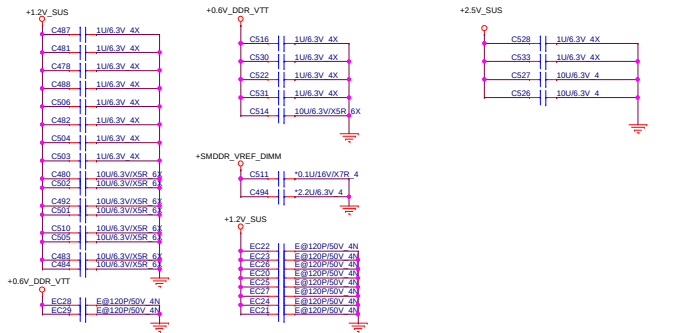
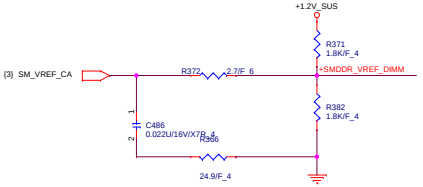


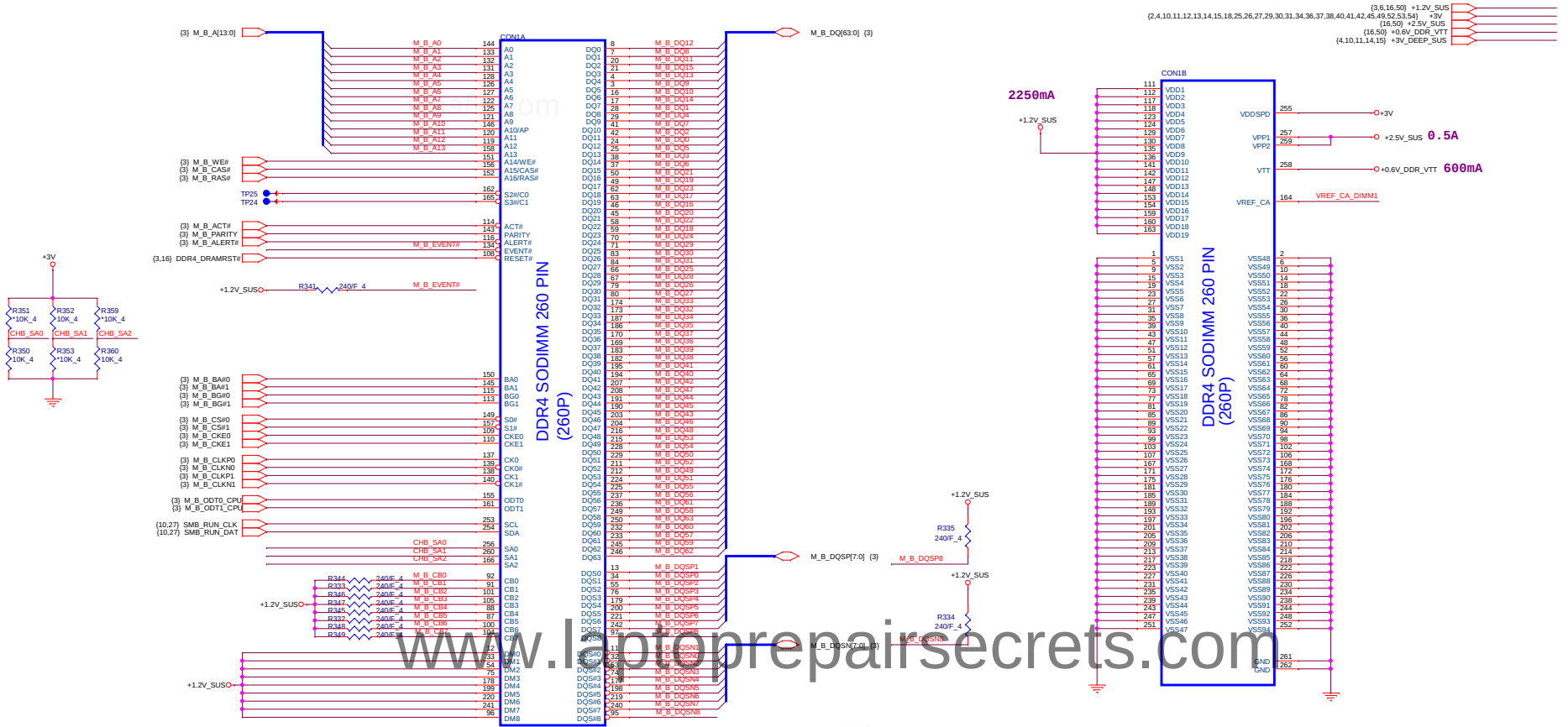
Place these Caps near Channel A





Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	DDR4 MEMORY DOWN	1A
Date: Friday, March 11, 2016	Sheet 16 of 61	



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PROJECT : LV6	
Size	Document Number: DDR4 DIMM1-RVS
Rev	1A
Date: Friday, March 11, 2016	Sheet 17 of 61

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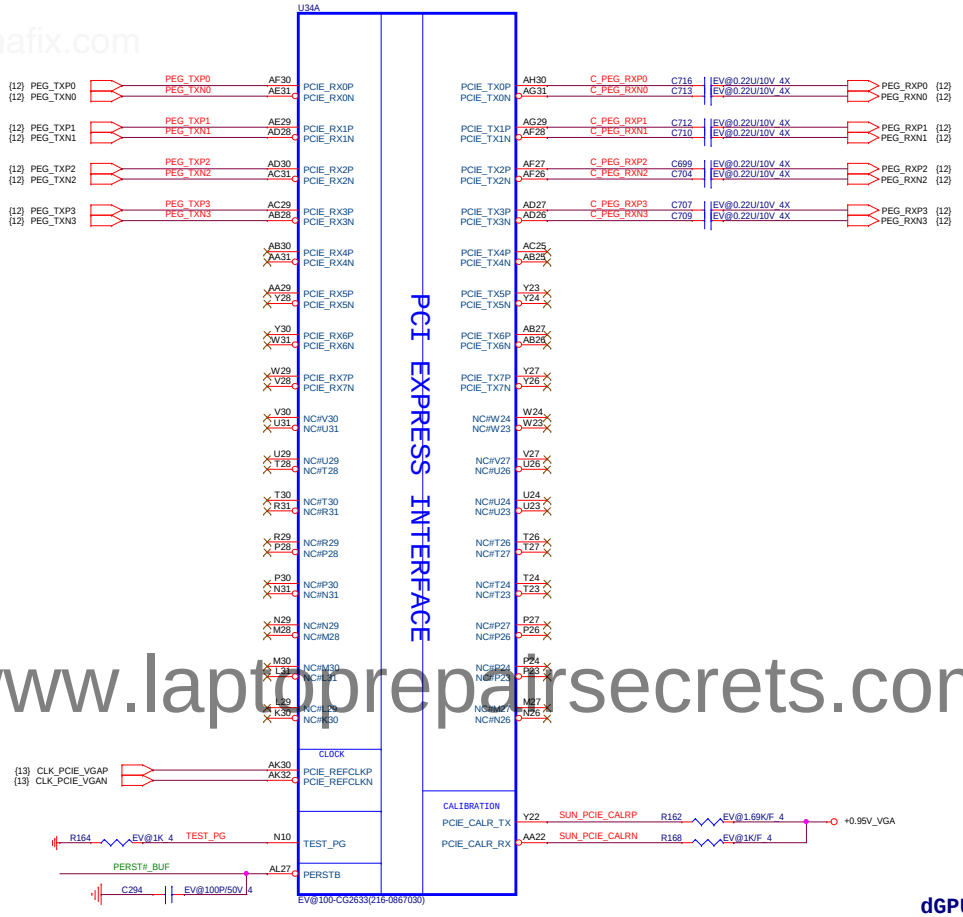

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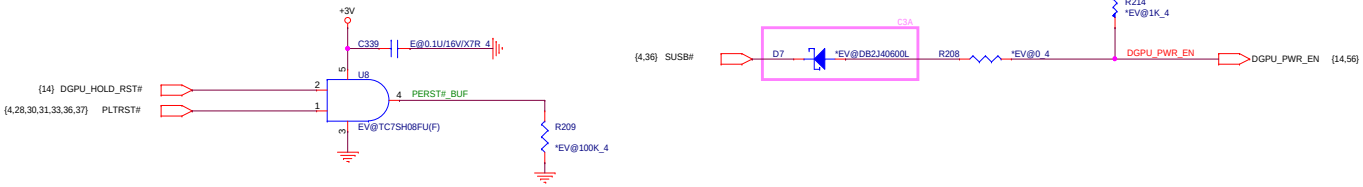
dGPU power enable



Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number	Rev
	JET_S3_PCIE_Interface	1A
Date: Friday, March 11, 2016	Sheet 18 of 61	

The SMBus slave ID is default 0x41

PU/PD

D3A

I2C

Level Shift

SVC	SVD	Output Voltage
0	0	1.1 Volts
0	1	1.0 Volts
1	0	0.9 Volts
1	1	0.8 Volts

R16M Boot

	R16M-M1-30	R16M-M2-50
PS0[5:1]	11001	11001
PS1[5:1]	11001	11001
PS2[5:1]	11000	11000
PS3[5:1]	11xxx	11xxx

PS_3[3:1]	Vendor	Type	Vendor P/N	R3pu	R3pd
011	Samsung- 2G	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	6.98K	4.99K
100	Hynix- 2G	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	4.53K	4.99K
101	Micro- 2G	256Mx16 *4, 900Mhz	MT41J256M16LY-091G:N	3.24K	5.62K

BIT[5:4]	C (nF)
00	680
01	82
10	10
11	NC

BIT[3:1]	Rpu	Rpd
000	NC	4750
001	8450	2000
010	4530	2000
011	6980	4990
100	4530	4990
101	3240	5620
110	3400	10000
111	4750	NC

M1 MLPS setting
M2 no mount

M1 ONLY: stuff Ra=> disable MLPS
stuff Rb=> enable MLPS

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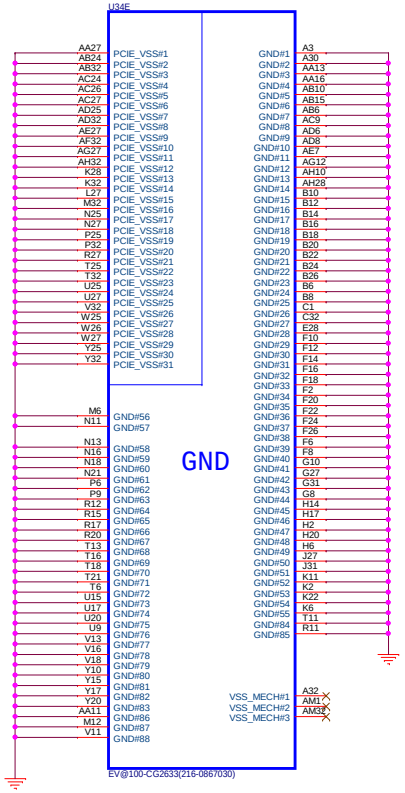
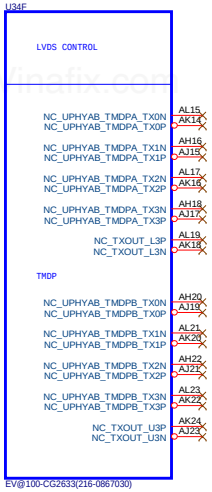
PROJECT : LV6
Size | Document Number: JET_S3_Main/DP PWR/Strap | Rev 1A
Date: Friday, March 11, 2016 | Sheet 19 of 61





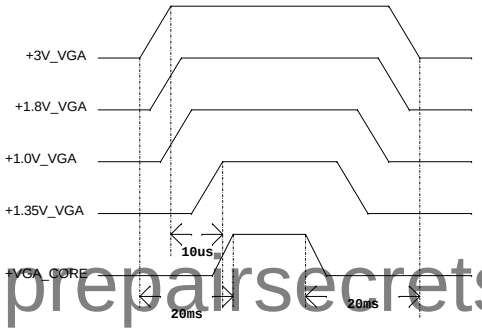
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

It is recommended that the 3.3-V rail ramp up first

The 3.3-V, 1.8-V, and 1.0-V rails must reach their ready state at least 10 µs before VDDC, VDDCI, and VMEMIO start to ramp up.

For power down, reversing the ramp-up sequence is recommended.

Power Up/Down Sequence



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PROJECT : LV6

Size	Document Number	Rev
	JET_S3_GND/LVDS	1A

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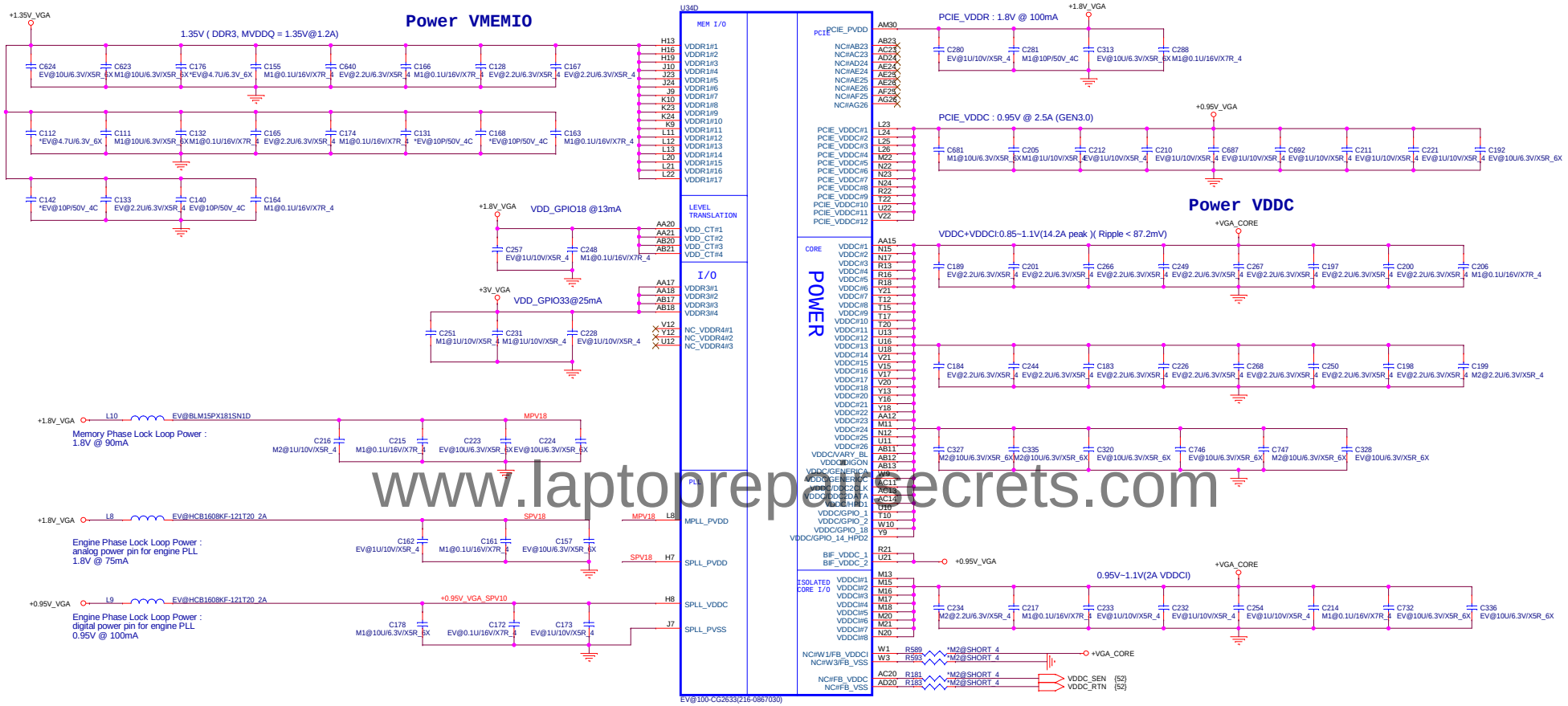

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PROJECT : LV6			
Size	Document Number		Rev
	JET_S3_Power		1A
Date: Friday, March 11, 2016		Sheet 21 of 61	

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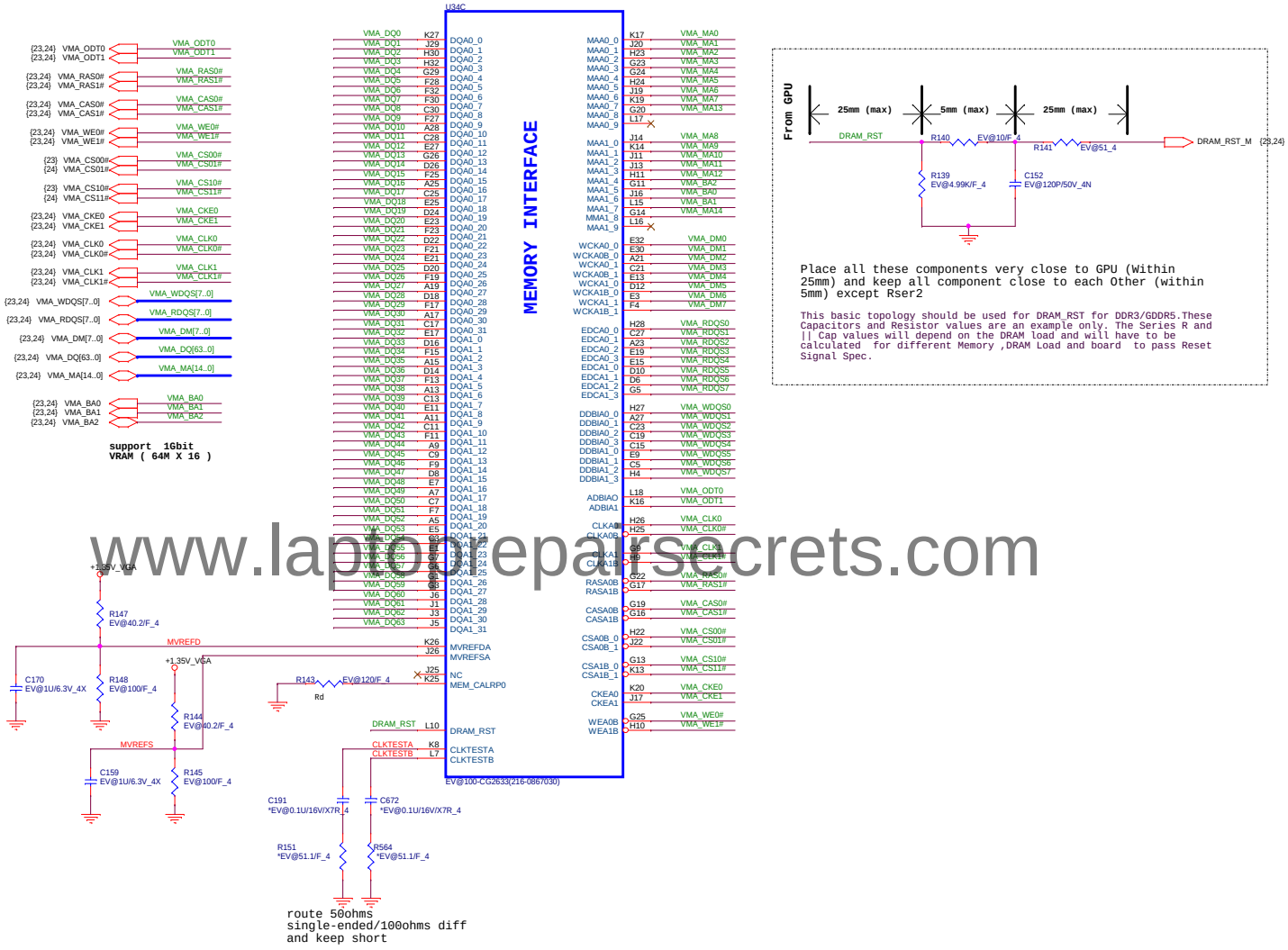

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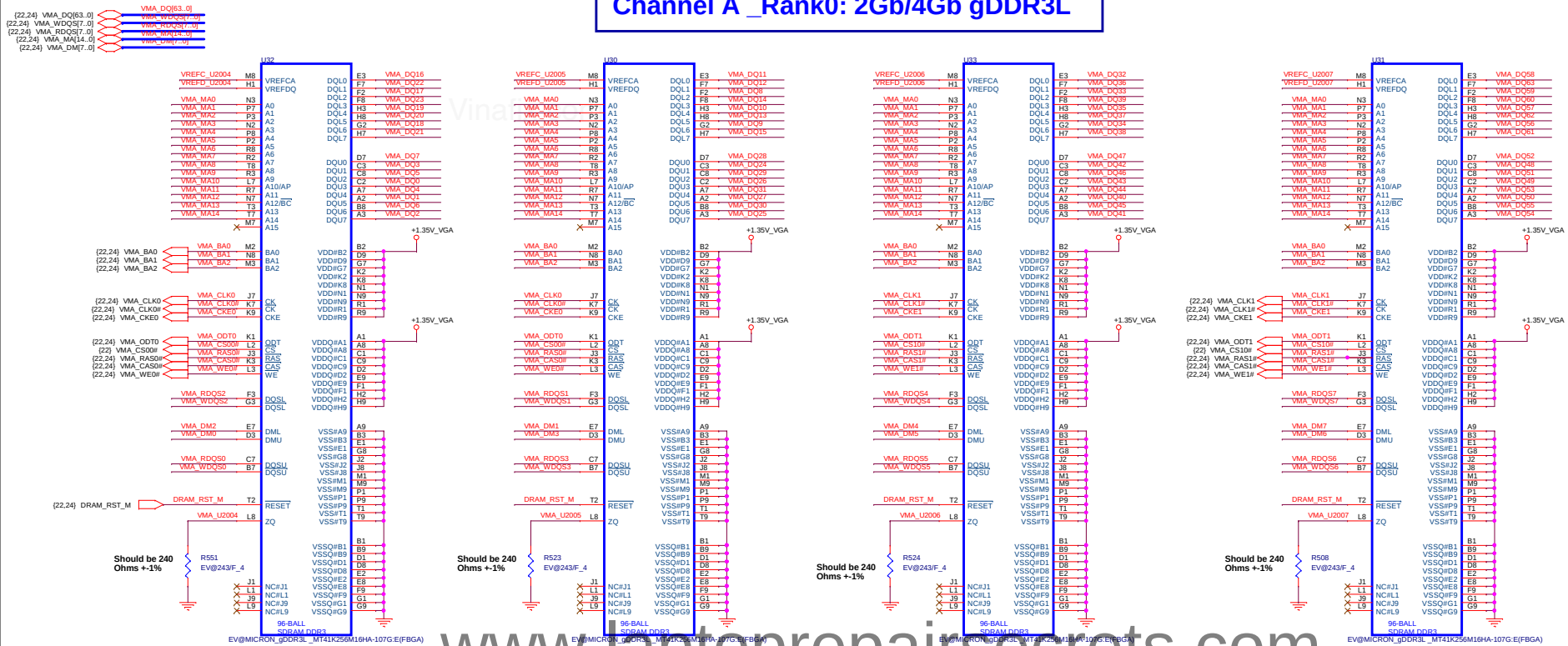
Quanta Computer Inc.			
PROJECT : LV6			
Size	Document Number		Rev
	JET_S3_MEM_Interface		1A
Date: Friday, March 11, 2016	Sheet 22 of 61		

Channel A _Rank0: 2Gb/4Gb gDDR3L



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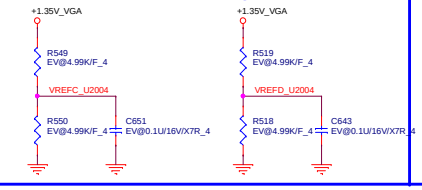
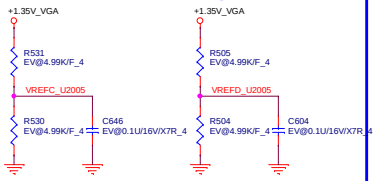
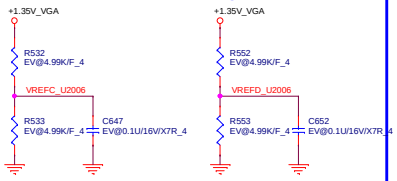
MEM Reference Voltage 1



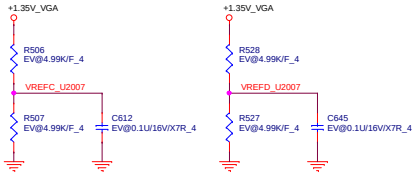
MEM Reference Voltage 2



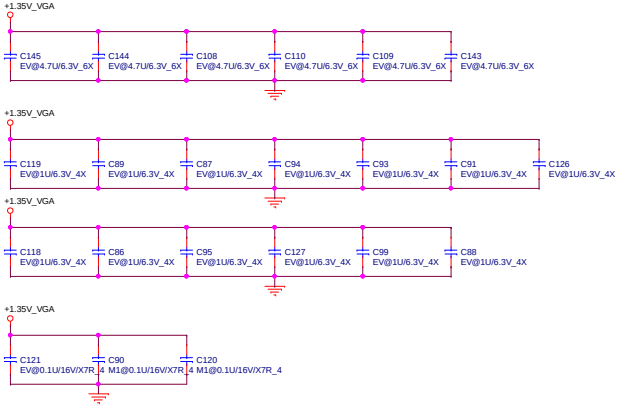
MEM Reference Voltage 3



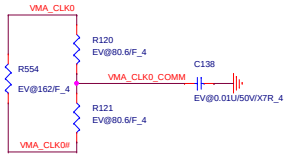
MEM Reference Voltage 4



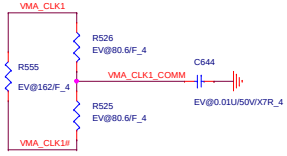
VRAM De-Coupling



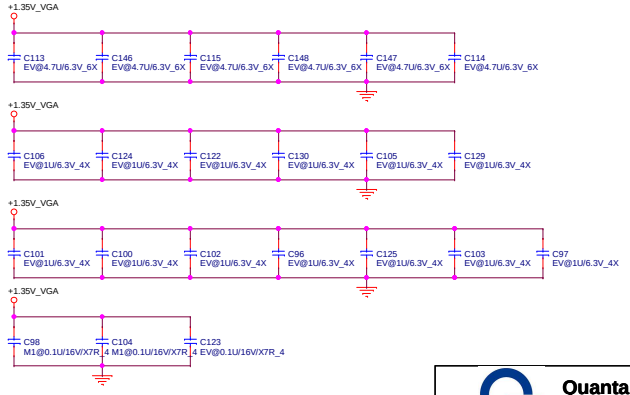
CLK-A0 Termination



CLK-A1 Termination



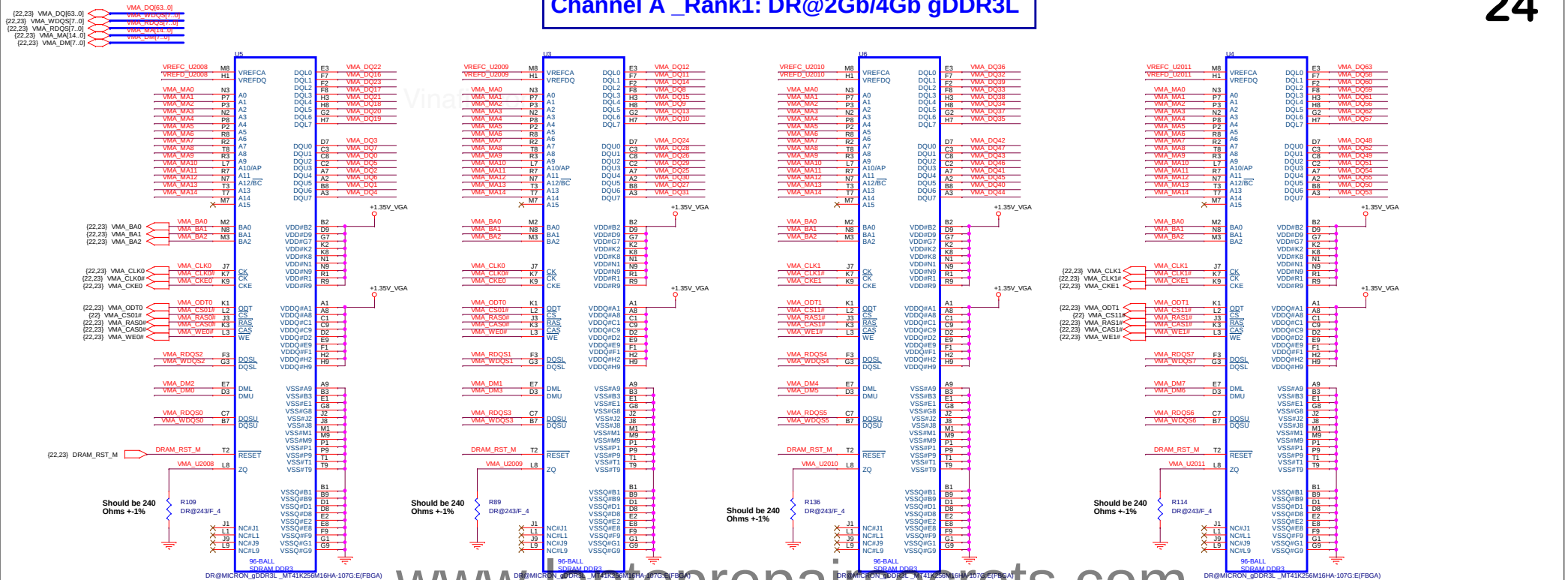
VRAM De-Coupling



Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	JET_S3_VRAM_DDR3 BGA96	1A
Date: Friday, March 11, 2016	Sheet 23 of 61	

Channel A _Rank1: DR@2Gb/4Gb gDDR3L



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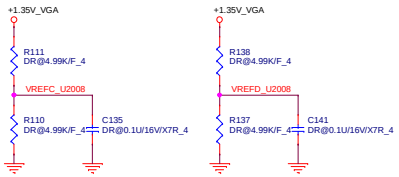
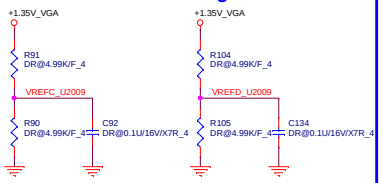
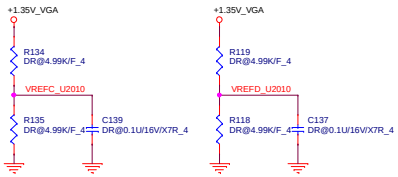
MEM Reference Voltage 1



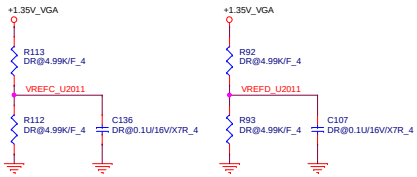
MEM Reference Voltage 2



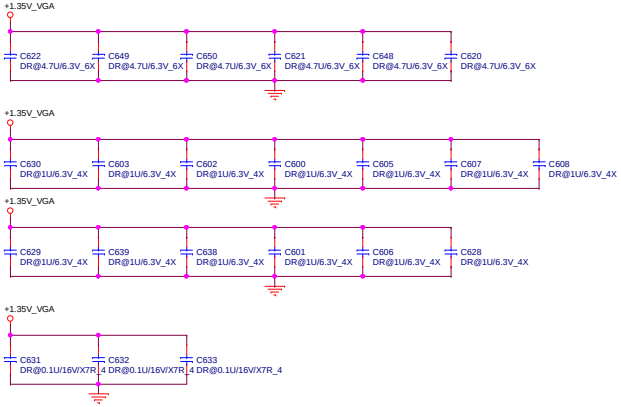
MEM Reference Voltage 3

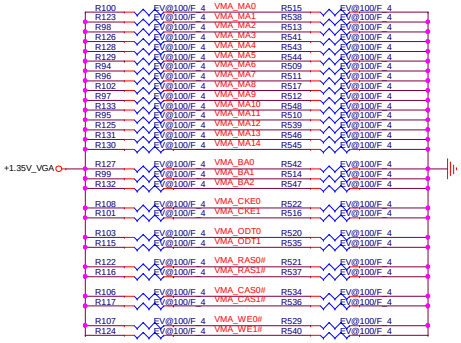


MEM Reference Voltage 4

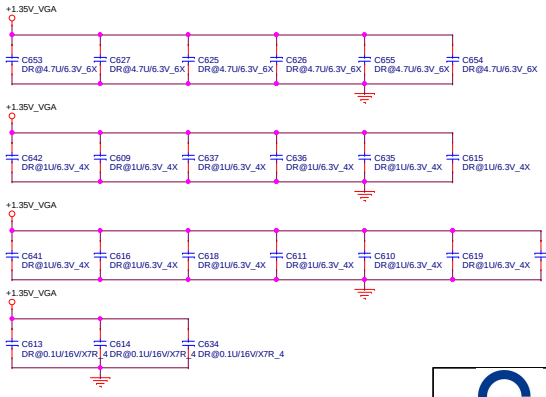


VRAM De-Coupling





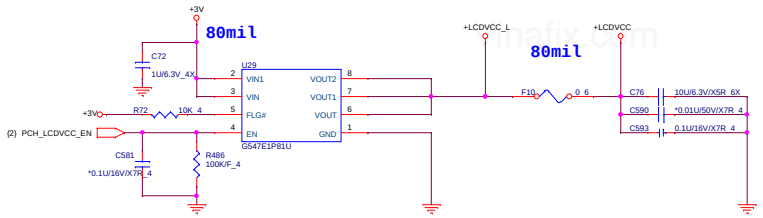
VRAM De-Coupling



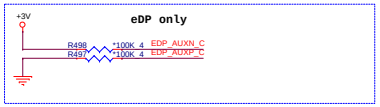
Quanta Computer Inc.
PROJECT : LV6

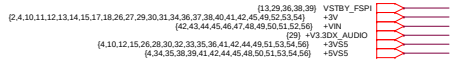
Size	Document Number	Rev
	JET_S3_Dual Rank VRAM	1A
Date: Friday, March 11, 2016	Sheet 24 of 61	

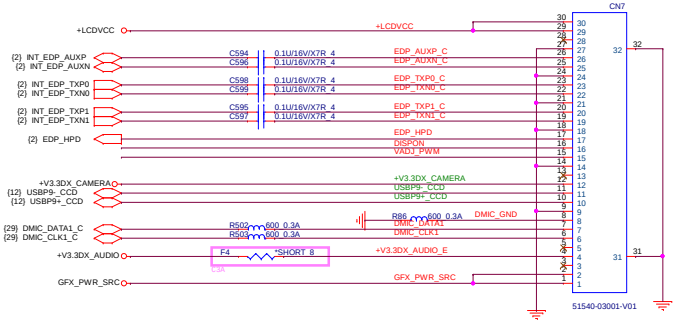
LCDVCC



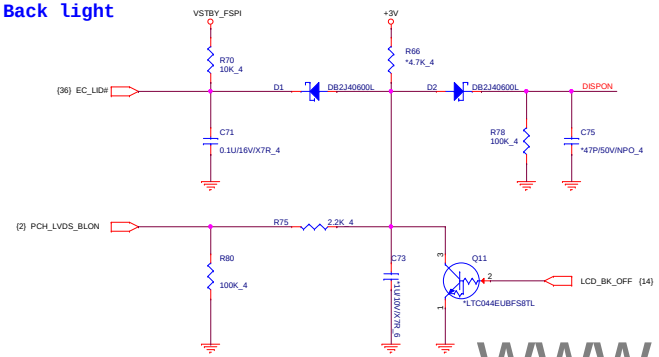
eDP only







Back light



For ESD

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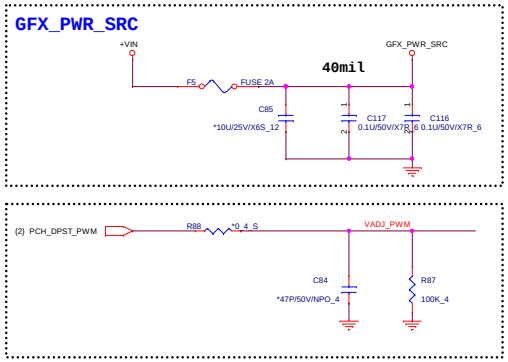
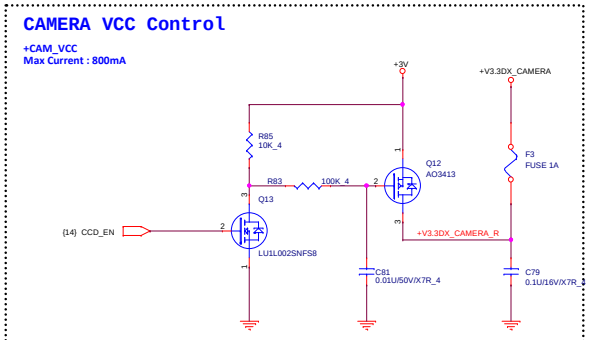
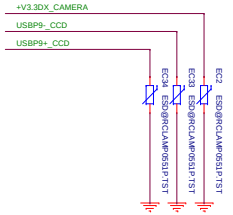
GFX_PWR_SRC



CAMERA VCC Control

+CAM_VCC
Max Current : 800mA





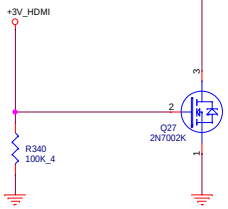
Quanta Computer Inc.
PROJECT : LV6

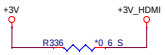
Size	Document Number	Rev
	LCD/CAMERA/MIC	1A

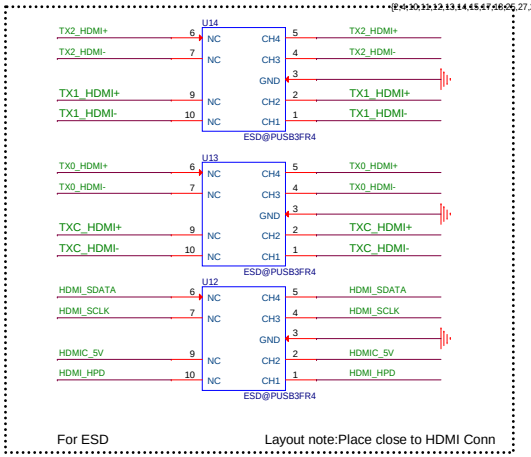
Date: Friday, March 11, 2016 Sheet 25 of 61

HDMI Conn <HDM>

HDMI-passive level shift <HDM>



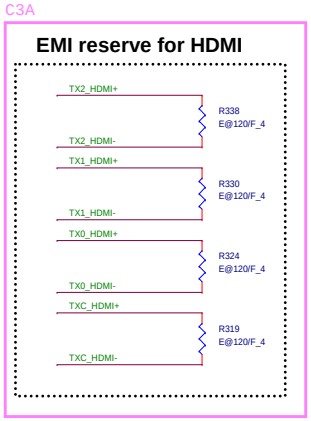




For ESD

Layout note:Place close to HDMI Conn

C3A



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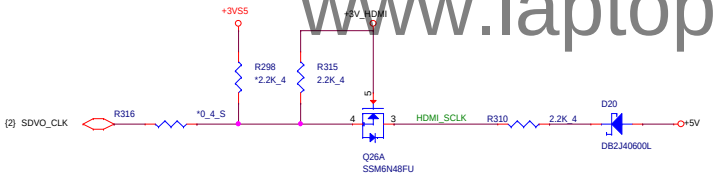
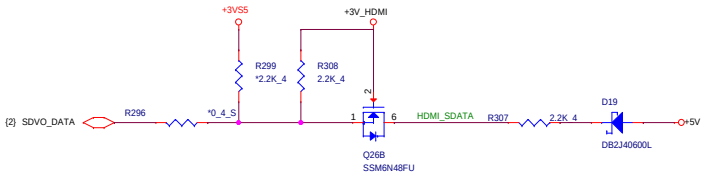
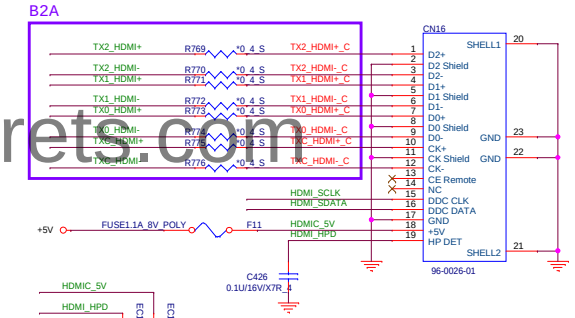
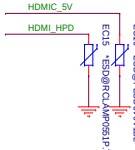
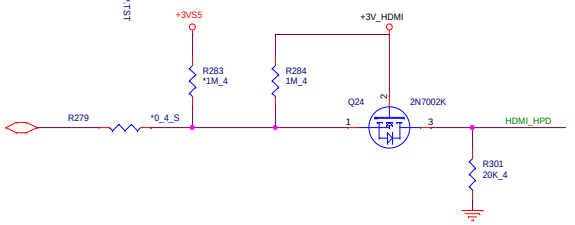




B2A







Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: HDMI CONN	Rev: 1A
Date: Friday, March 11, 2016	Sheet 26 of 61	

CRT Conn <CRT>

+5V {26,29,31,37,39,52,53}
+3V {2,4,10,11,12,13,14,15,17,18,25,26,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54}

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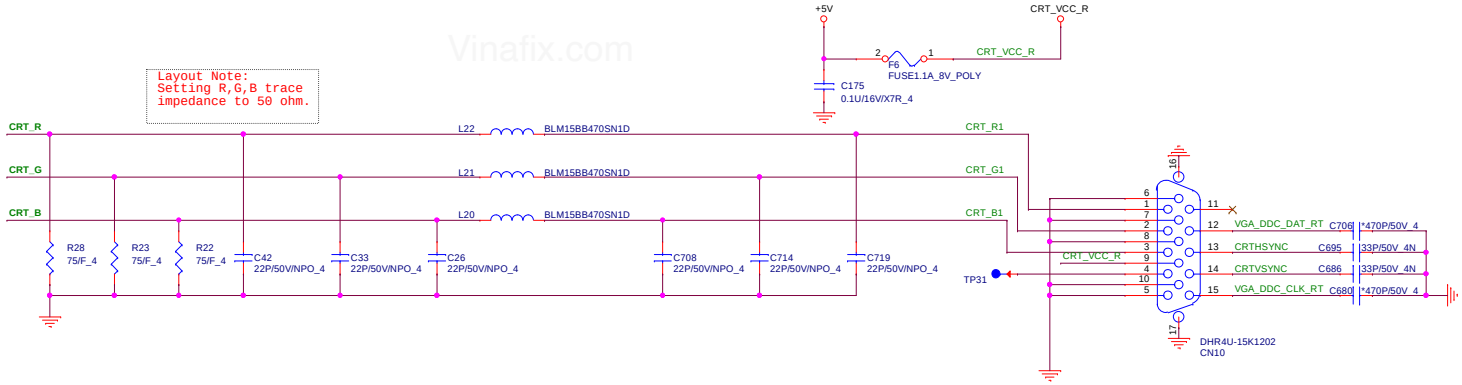
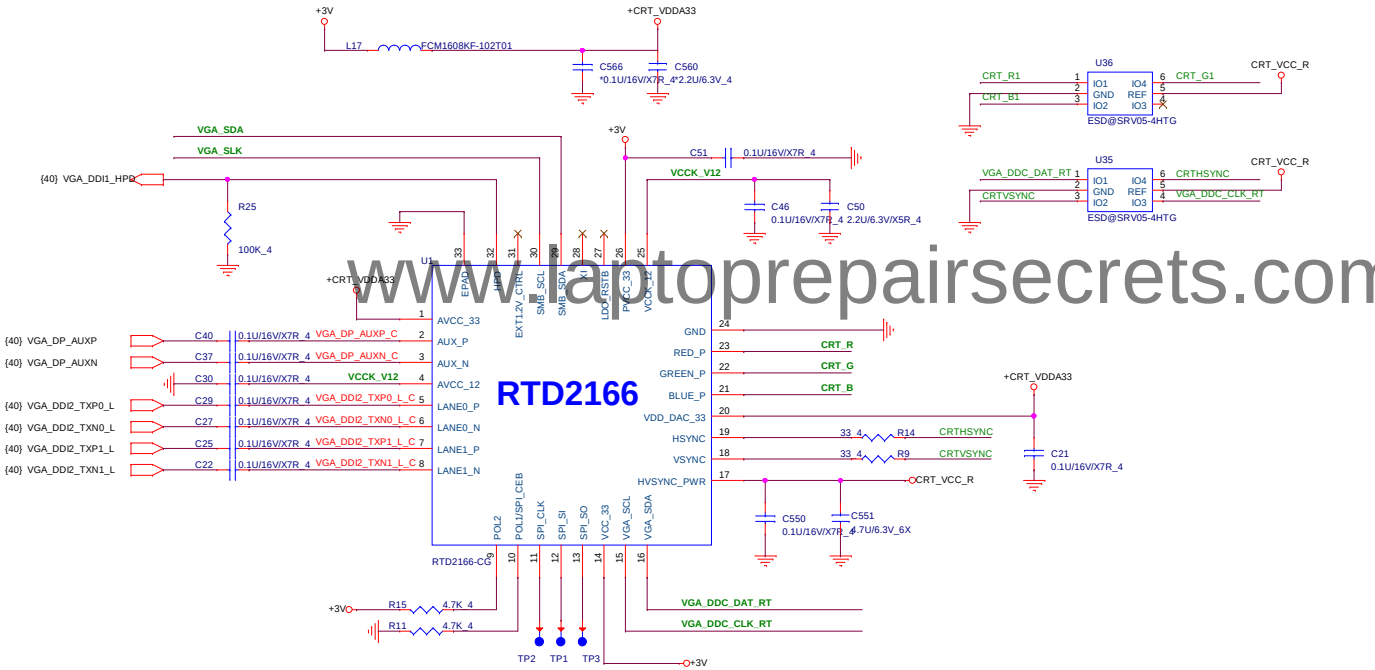
Layout Note:
Setting R,G,B trace impedance to 50 ohm.





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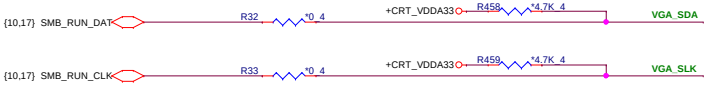

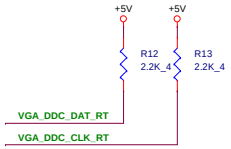

Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number	Rev
	DP to CRT(RTD2166-CG)	1A
Date: Friday, March 11, 2016	Sheet 27 of 61	

TPM <TPM>

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{4,10,12,15,26,30,32,33,35,36,41,42,44,49,51,53,54,56}
+3V
+3VS5

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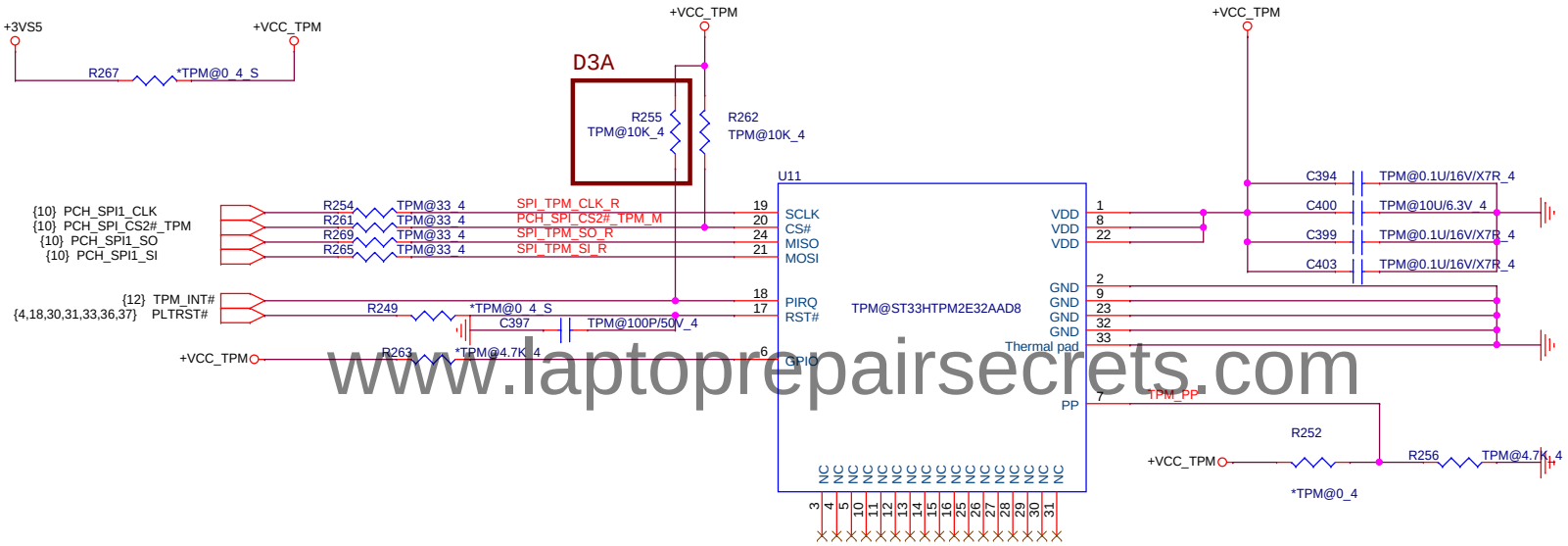

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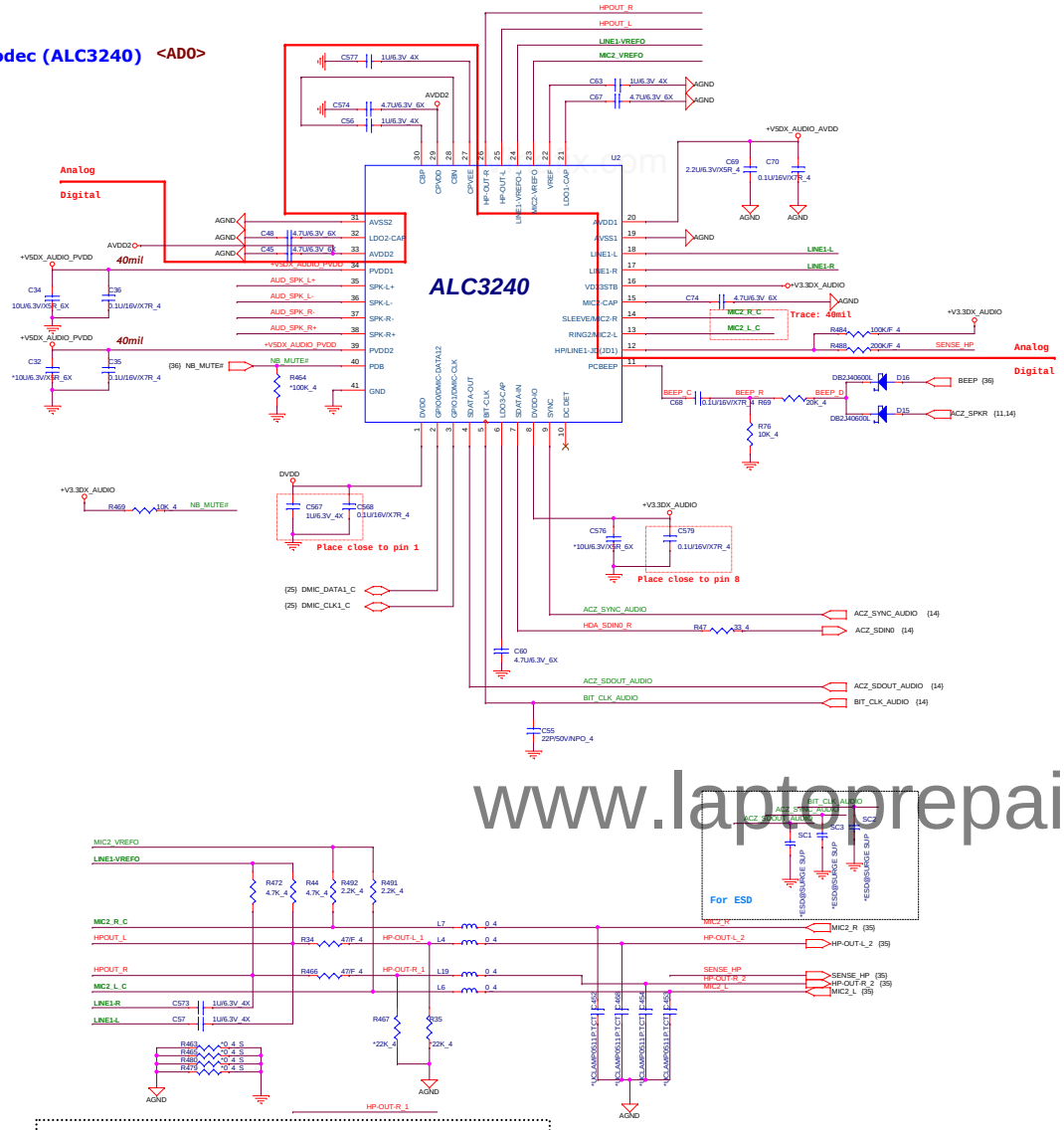
Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: TPM	Rev: 1A
Date: Friday, March 11, 2016	Sheet 28 of 61	

Codec (ALC3240) <ADO>



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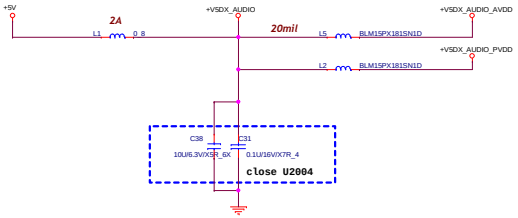
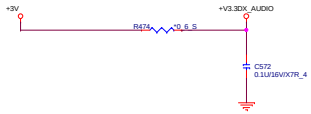
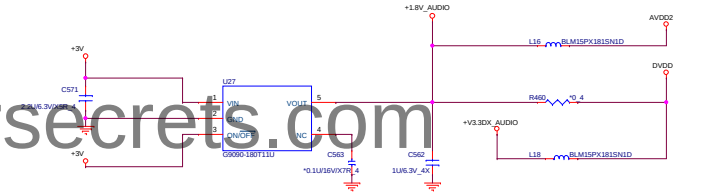
CODEC 5V POWER



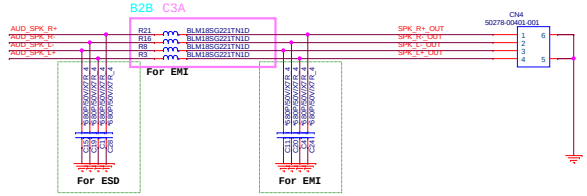
+3.3V_AUDIO_CODEC

Max Current : 419mA



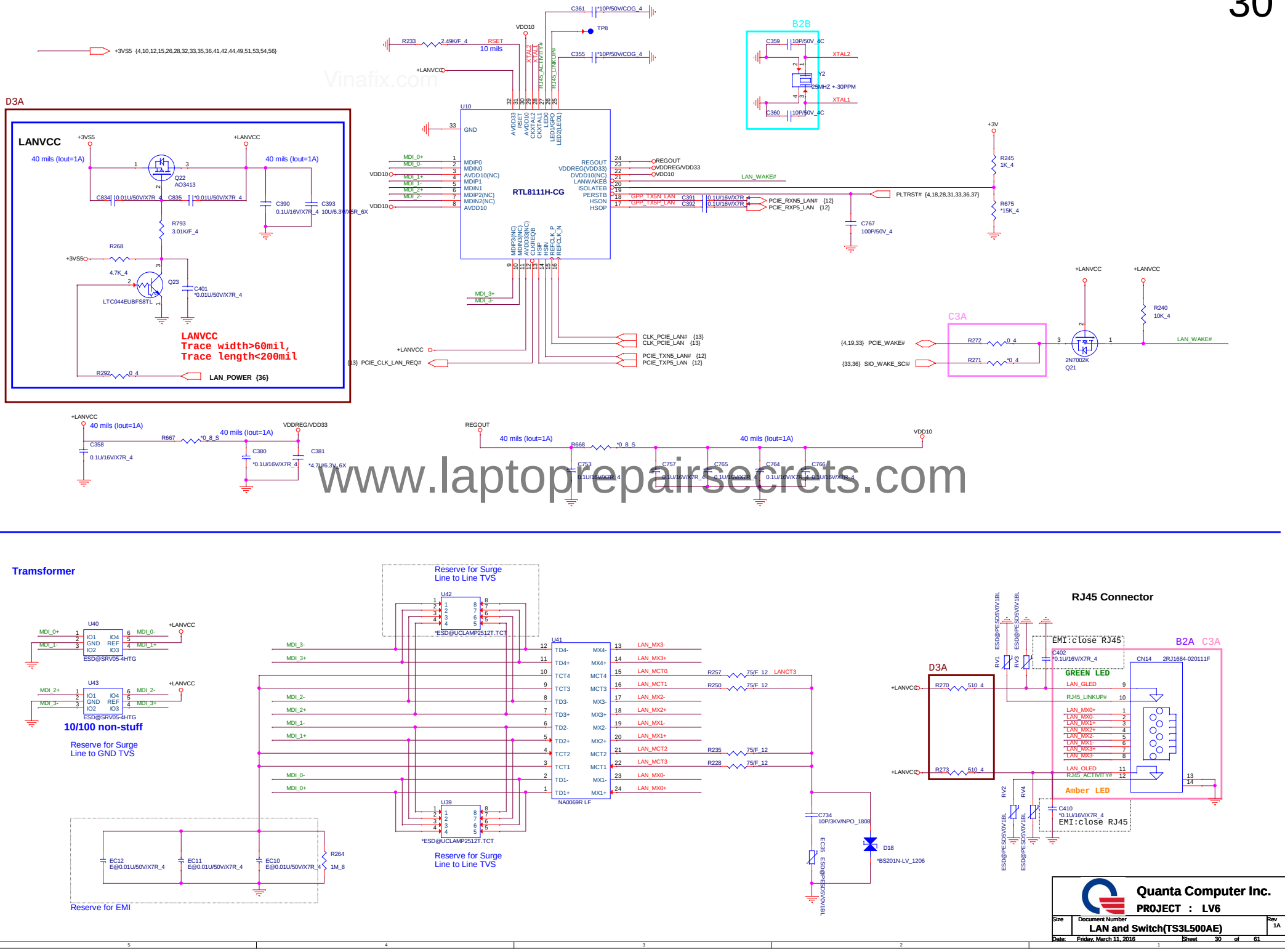


INT Speaker



Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: Audio(ALC3240)	Rev: 1A
Date: Friday, March 11, 2016	Sheet 29 of 61	

LAN LDO <LAN>



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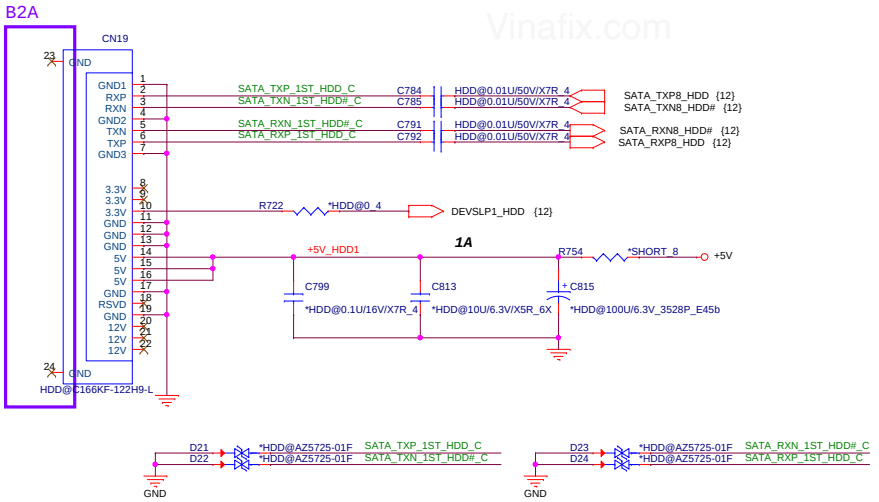
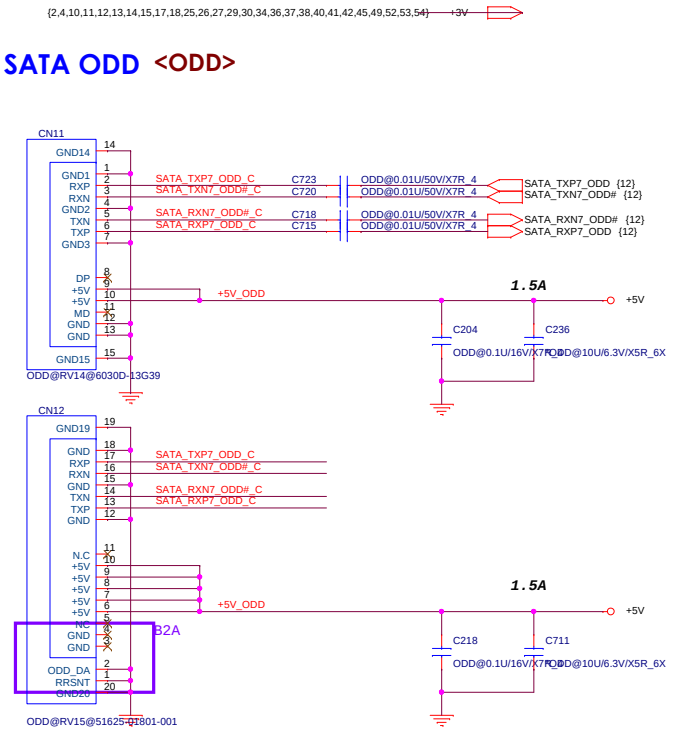
Tramsformer

Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number	Rev
	LAN and Switch(TS3L500AE)	1A
Date: Friday, March 11, 2016	Sheet 30 of 61	

SATA HDD <HDD>



SATA ODD <ODD>



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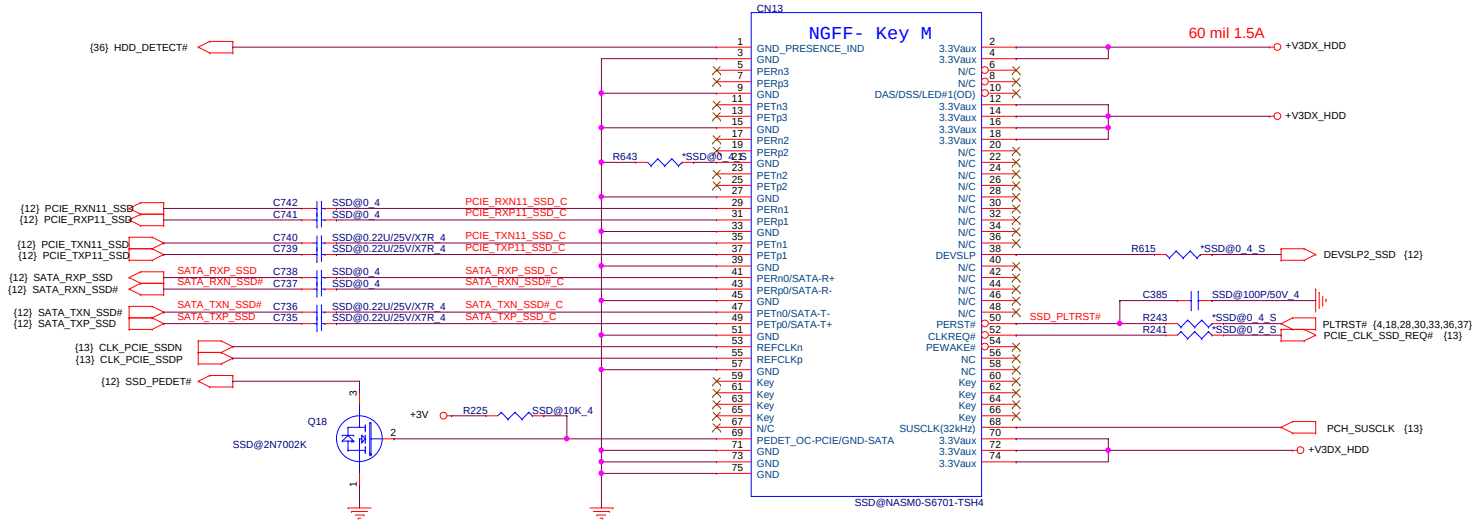
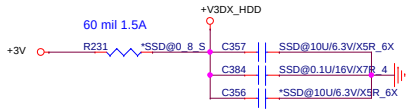
SSD M.2 <HDD>



DC Current rating: 3 A (MAX)



Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	HDD/ODD/SSD	1A

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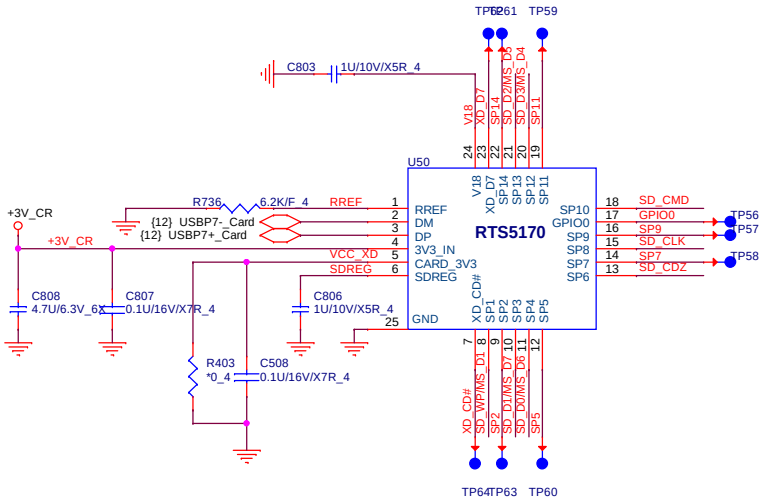
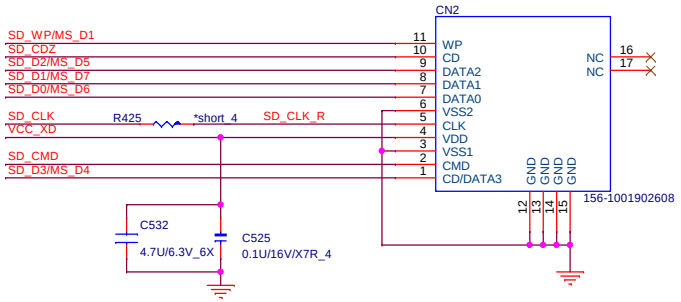
Vinafix.com





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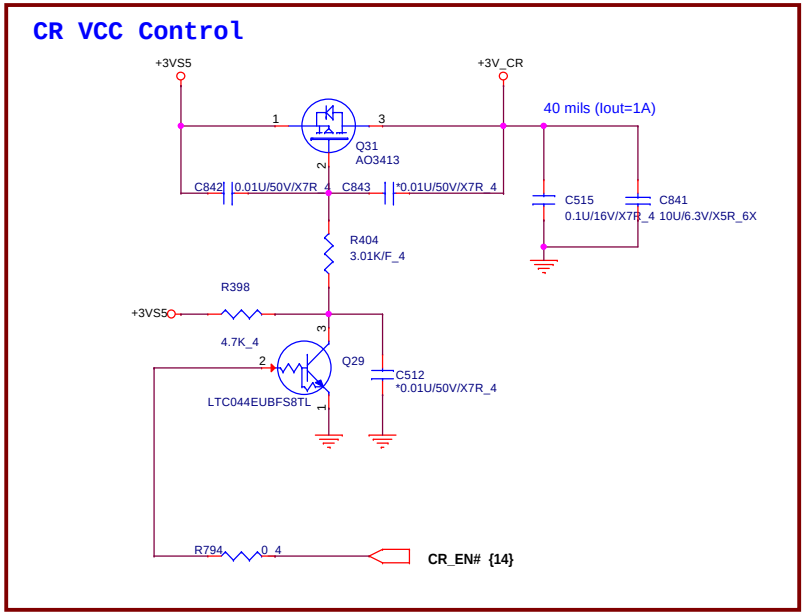
D3A

CR VCC Control



Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: Card Reader	Rev: 1A
Date: Friday, March 11, 2016	Sheet 32 of 61	

NGFF WiFi/BT connector
M.2 2230

<WIF>

33

{4,10,12,15,26,28,30,32,35,36,41,42,44,49,51,53,54,56} +3VS5
{13,25,29,36,38,39} VSTBY_FSPI

+3.3V_NGFF_WLAN

CN6

NGFF-KEY-E

1	GND	3.3Vaux	2
3	USB_D+	3.3Vaux	4
5	USB_D-	LED#1 (OD)	6
7	GND	PCM_CLK (0/1.8V)	8
9	SDIO CLK(O)(0/1.8V)	PCM_SYNC (0/1.8V)	10
11	SDIO CMD(IO)(0/1.8V)	PCM_IN (0/1.8V)	12
13	SDIO DAT0(IO)(0/1.8V)	PCM_OUT (0/1.8V)	14
15	SDIO DAT1(IO)(0/1.8V)	LED#2 (OD)	16
17	SDIO DAT2(IO)(0/1.8V)	GND	18
19	SDIO DAT3(IO)(0/1.8V)	UART Wake(0/3.3V)	20
21	SDIO Wake(I)(0/1.8V)	UART Rx (0/1.8V)	22
23	SDIO Reset(O)(0/1.8V)	Key	24
25	Key	Key	26
27	Key	Key	28
29	Key	Key	30
31	Key	Key	32
33	Key	UART Tx (0/1.8V)	34
35	GND	UART CTS (0/1.8V)	36
37	PETp0	UART RTS (0/1.8V)	38
39	PETn0	RESERVED	40
41	GND	RESERVED	42
43	PERp0	RESERVED	44
45	PERn0	COEX3(?)(0/1.8V)	46
47	GND	COEX2(?)(0/1.8V)	48
49	REFCLKP0	COEX1(?)(0/1.8V)	50
51	REFCLKN0	SUSCLK(32kHz)(0/3.3V)	52
53	GND	PERST0#(0/3.3V)	54
55	CLKREQ0#(0/3.3V)	W_Disable#2(0/3.3V)	56
57	PEWake0#(0/3.3V)	W_Disable#1(0/3.3V)	58
59	GND	I2C DATA(0/3.3)	60
61	Reserved/PETp1	I2C CLK(0/3.3)	62
63	Reserved/PETn1	ALERT(0/3.3)	64
65	GND	RESERVED	66
67	Reserved/PERp1	RESERVED	68
69	Reserved/PERn1	RESERVED	70
71	GND	RESERVED	72
73	RESERVED	3.3Vaux	74
75	RESERVED	3.3Vaux	
	GND		

NASE0-S6701-TS48

{12} USBP8+_BT
{12} USBP8-_BT

{12} PCIE_TXP6_WLAN
{12} PCIE_TXN6_WLAN#
{12} PCIE_RXP6_WLAN
{12} PCIE_RXN6_WLAN#
{13} CLK_PCIE_WLANP
{13} CLK_PCIE_WLANN
{13} PCIE_CLK_WLAN_REQ#
MINICARD_PME#

{10} DEBUG_LCLKOUT
{10,36} LPC_LFRAME#
*NMP@0_4_S R500 DEBUG_LCLKOUT_L
*NMP@0_4_S R501 LPC_LFRAME#_R

R57 *0_4_S CL_RST# {10}
R67 *0_4_S CL_DATA {10}
R73 *0_4_S CL_CLK {10}

WLANSUSCLK
PLTRST#
BT_OFF_R#
WLAN_OFF_R#
TP30
PLTRST# {4,18,28,30,31,36,37}
C78 100P/50V_4

LPC_LAD0_R R494 *NMP@0_4_S LPC_LAD0 {10,36}
LPC_LAD1_R R495 *NMP@0_4_S LPC_LAD1 {10,36}
LPC_LAD2_R R496 *NMP@0_4_S LPC_LAD2 {10,36}
LPC_LAD3_R R499 *NMP@0_4_S LPC_LAD3 {10,36}

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C3A

+3.3V_NGFF_WLAN +3.3V_NGFF_WLAN
R39 10K_4
{4,19,30} PCIE_WAKE# R54 0_4
{30,36} SIO_WAKE_SCI# R60 *0_4
2N7002K Q7
MINICARD_PME#

{12} WLAN_OFF#
{14} BT_RADIO_DIS#
D3 DB2J40600L
D6 DB2J40600L
R79 10K_4 +3.3V_NGFF_WLAN
R77 10K_4
WLAN_OFF_R#
BT_OFF_R#

D3A

+3VS5
+3.3V_ NGFF_WLAN
Max Current : 1000mA
+3.3V_NGFF_WLAN
40 mils (Iout=1A)
40 mils (Iout=1A)
Q6 AO3413
C58 0.01U/50V/X7R_4 C836 *0.01U/50V/X7R_4
C47 0.1U/16V/X7R_4 C838 10U/6.3V/X5R_6X
R55 3.01K/F_4
R68
{4} SLP_WLAN# D4 DB2J40600L
{36} EC_WLAN_EN D5 *DB2J40600L
+3VS5
4.7K_4
Q8 LTC044EUBFS8TL
C66 *0.01U/50V/X7R_4

+3.3V_NGFF_WLAN Place caps close to connector.
C39 0.1U/16V/X7R_4
C83 0.047U/25V/X7R_4
C44 0.1U/16V/X7R_4
C43 0.047U/25V/X7R_4
C52 4.7U/6.3V_6X

Quanta Computer Inc.
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	Wifi/BT NGFF	1A
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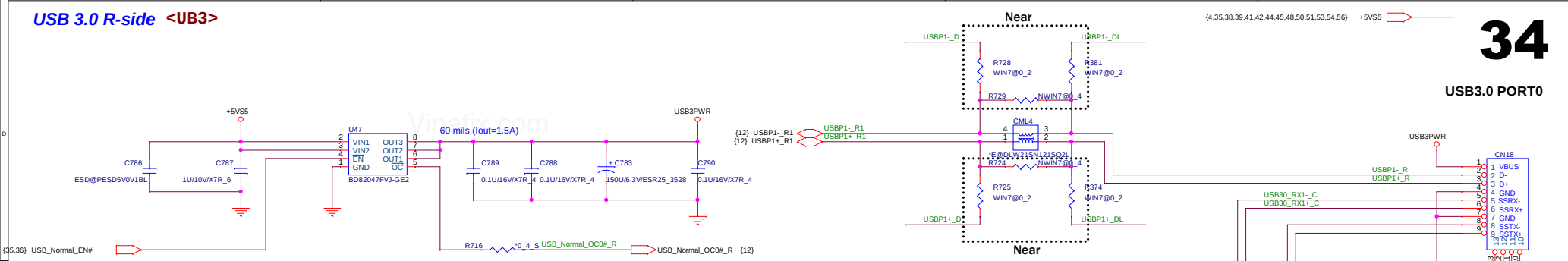
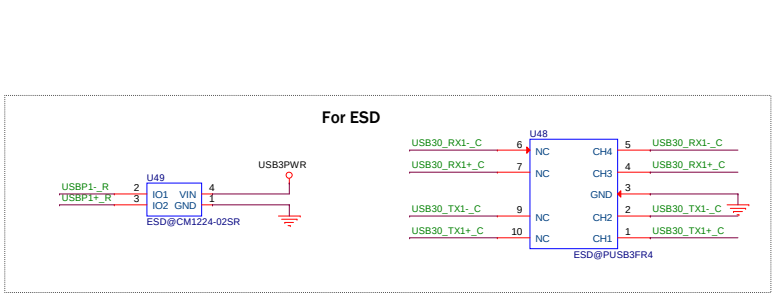
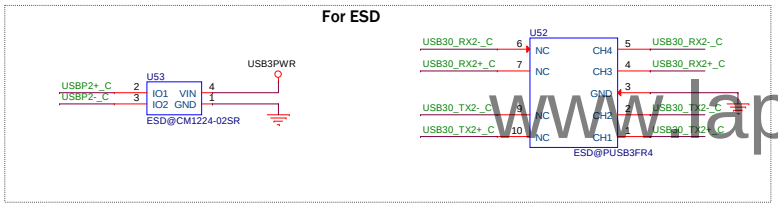
USB 3.0 R-side <UB3>

34

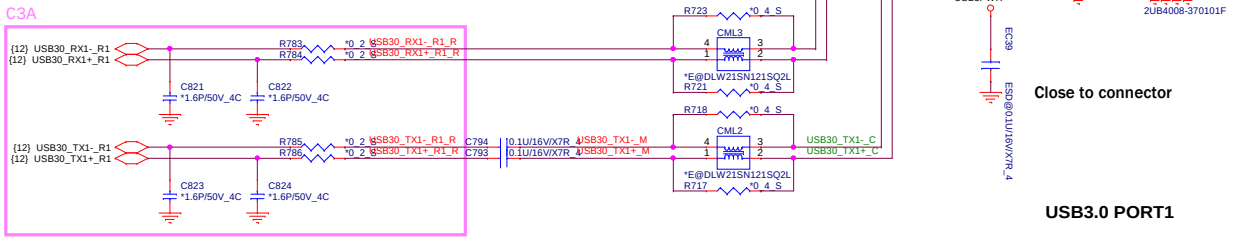
USB3.0 PORT0





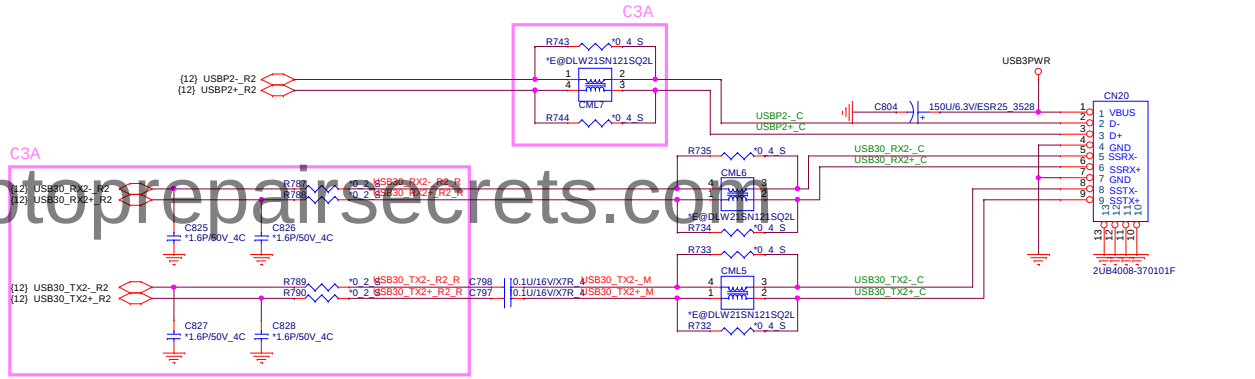


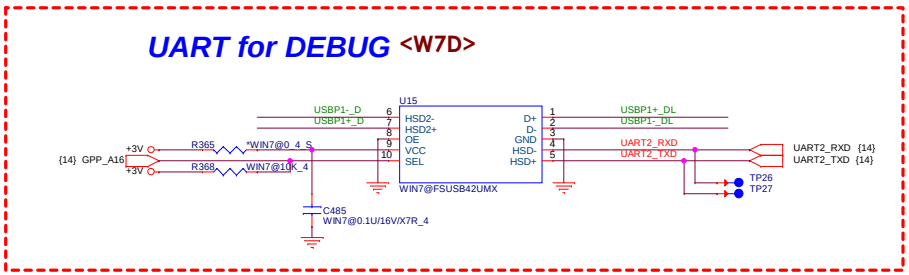
C3A

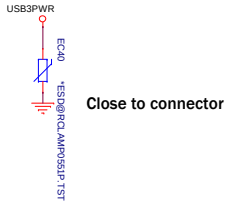


USB3.0 PORT1

C3A







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	USB3x2	1A

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USB Sleep&Charger <UBC> <UB2>

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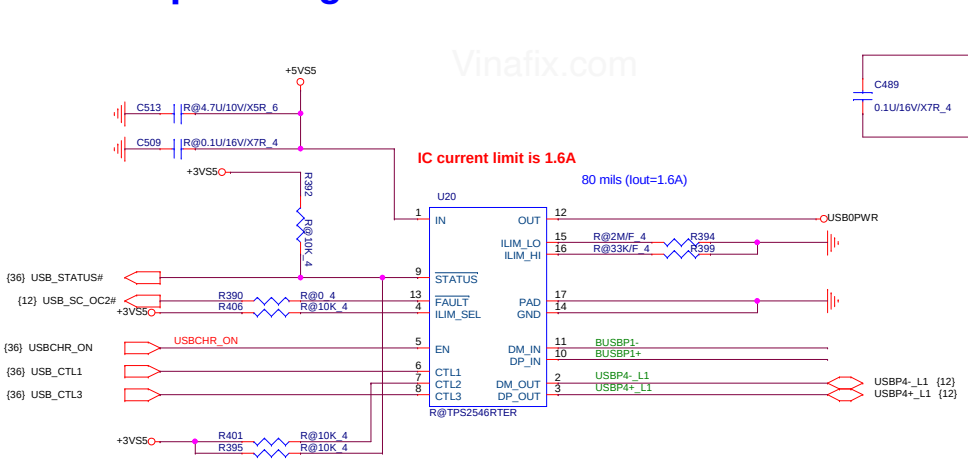
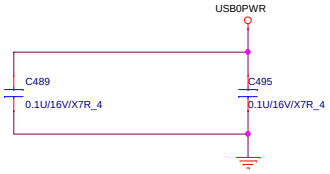
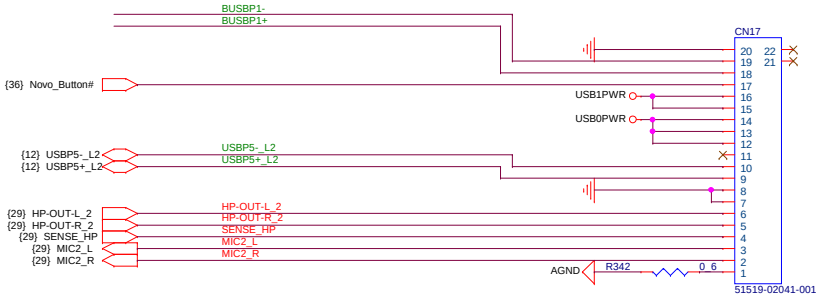
{4,34,38,39,41,42,44,45,48,50,51,53,54,56} +5VS5
{4,10,12,15,26,28,30,32,33,36,41,42,44,49,51,53,54,56} +3VS5

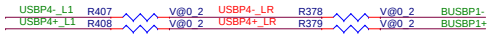


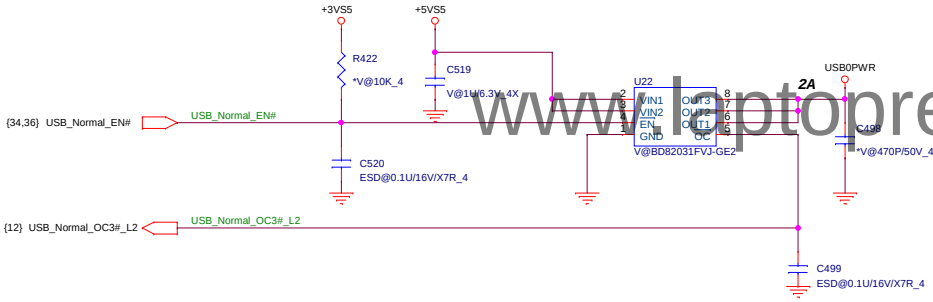


USB3.0 (with AOU5)



USB2.0 Power SW <UB2>





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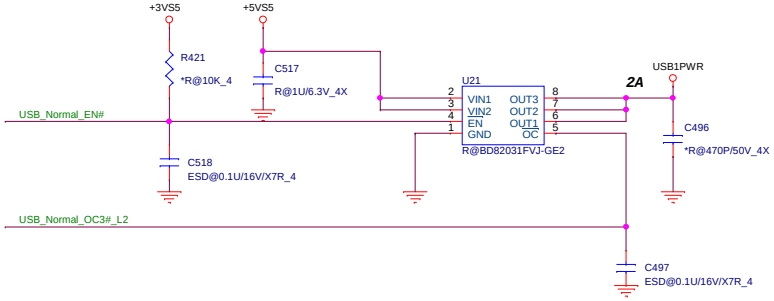
USB2.0 Power SW <UB2>



Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: S&C/ USB2 (AOU5)	Rev: 1A
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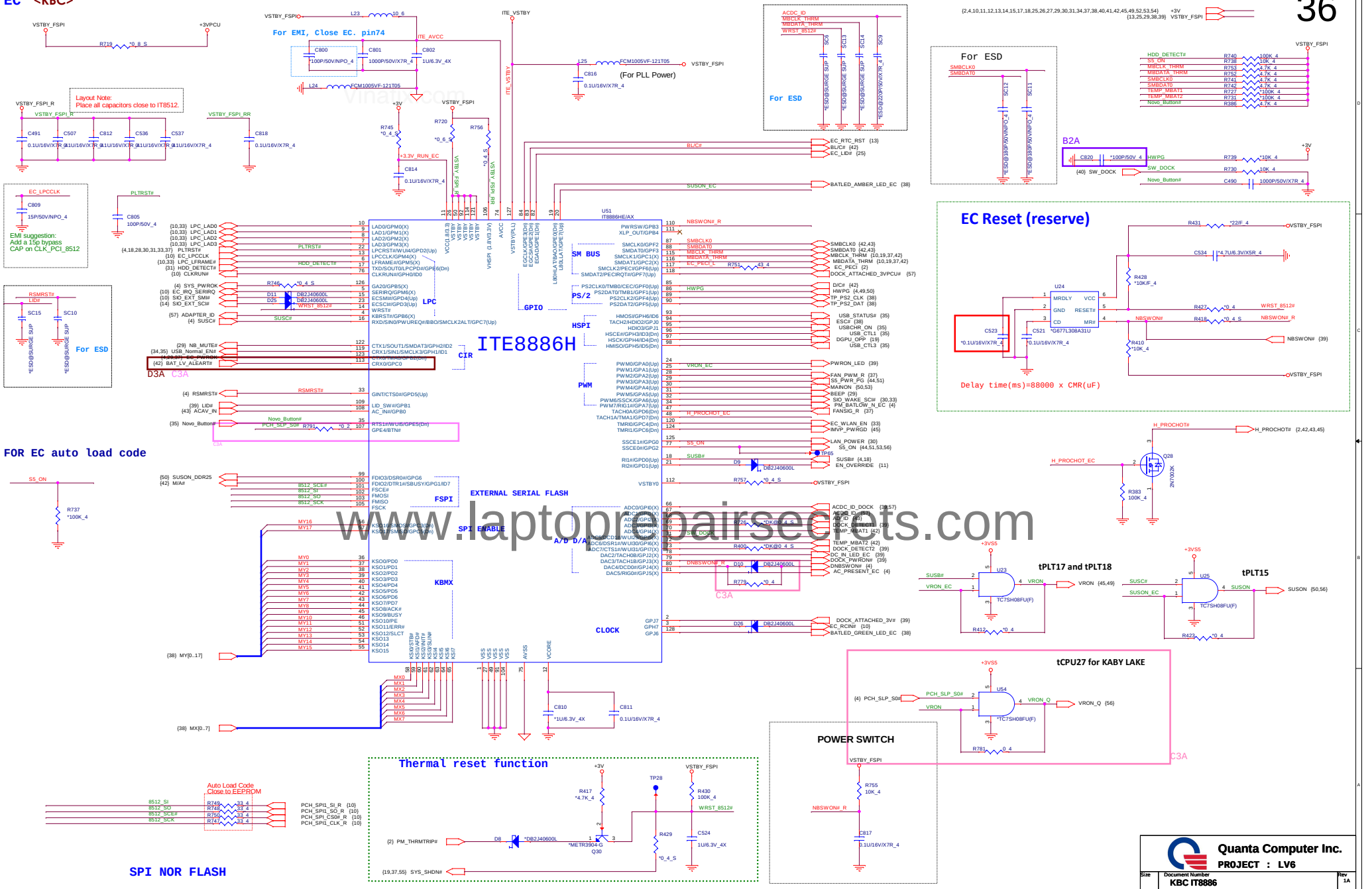
EC <KBC>



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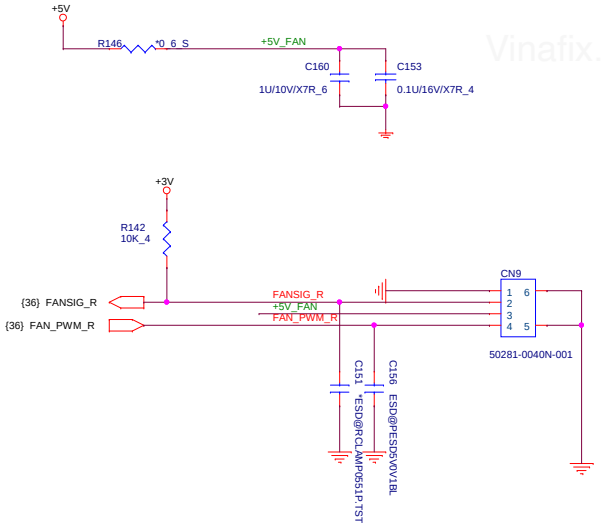
FAN CONN



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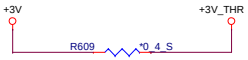
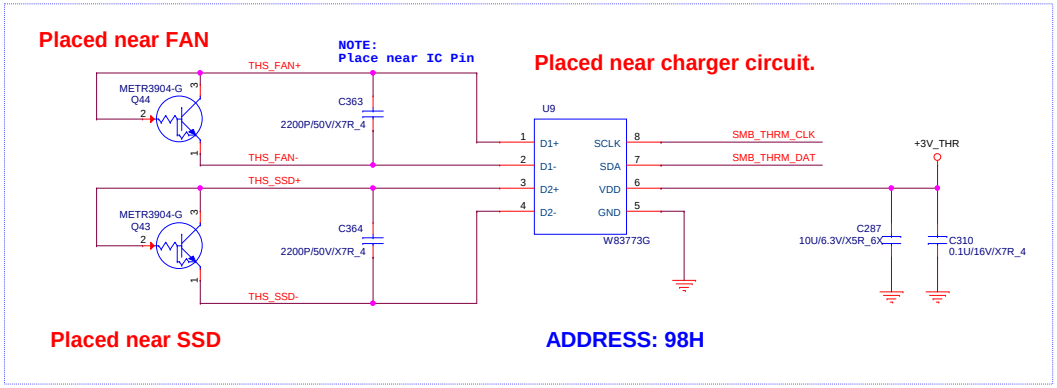
Thermal Sensor

{2,4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,38,40,41,42,45,49,52,53,54} +3V
{26,27,29,31,39,52,53} +5V





CPU PTC circuit

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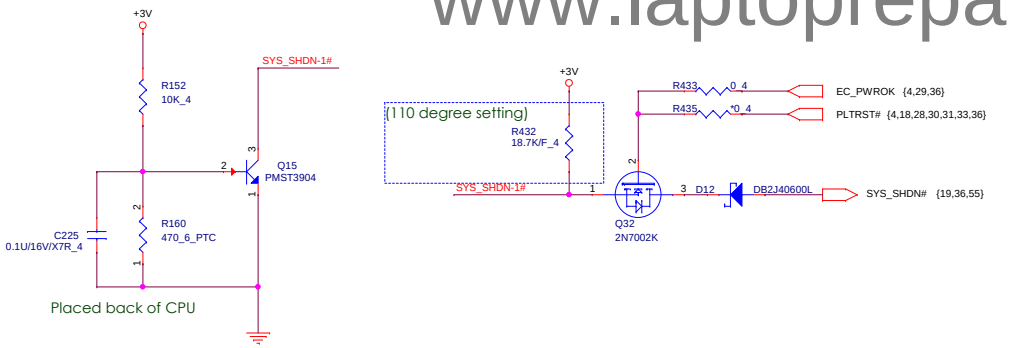

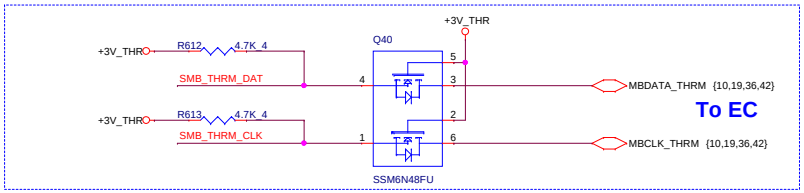

Quanta Computer Inc.
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	Thermal	1A
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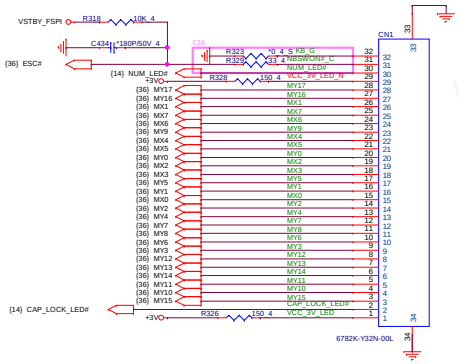
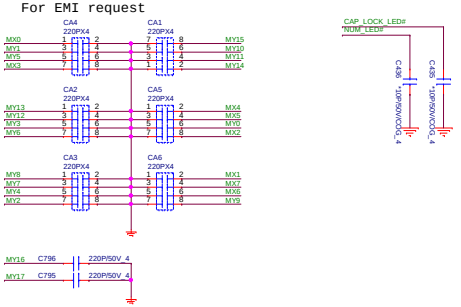
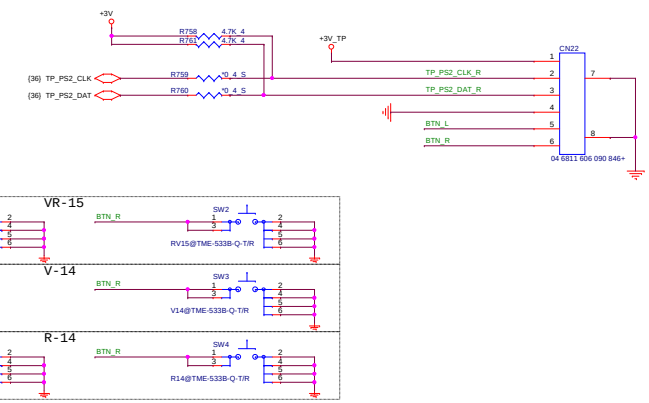
INT KeyBoard <KBC>



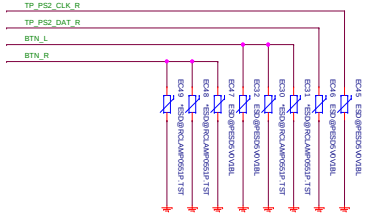
For EMI request



TP Control <TPD>

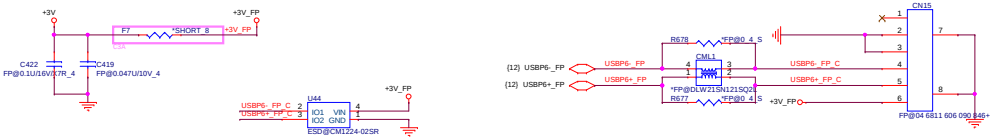


Touch pad

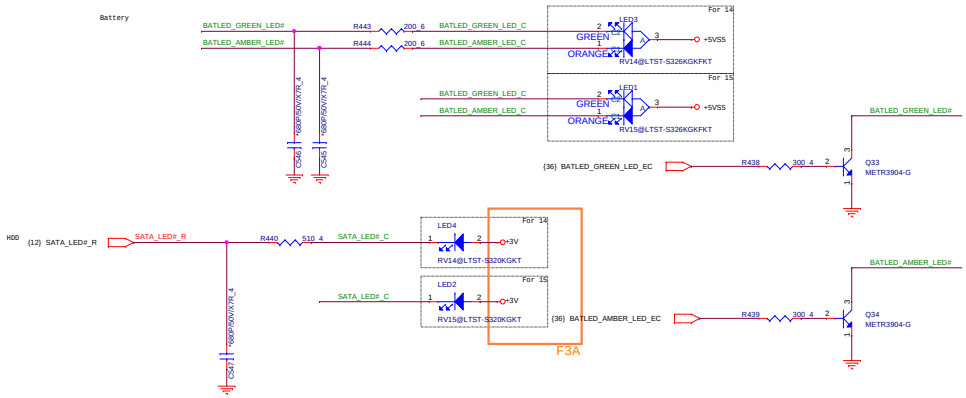


Finger Print <FPD>

USB INTERFACE



LED <UIF>



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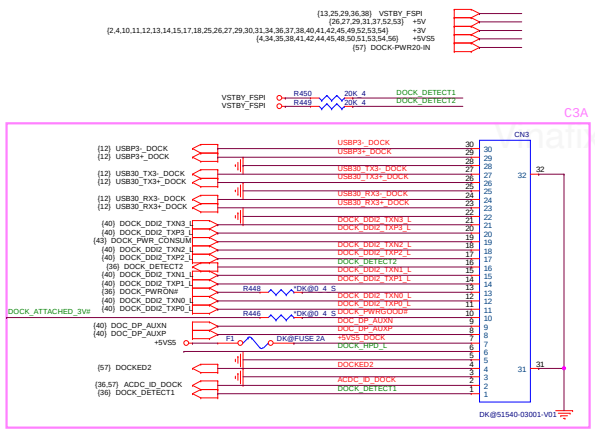
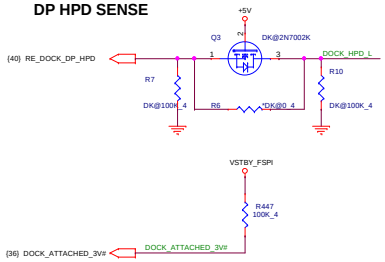
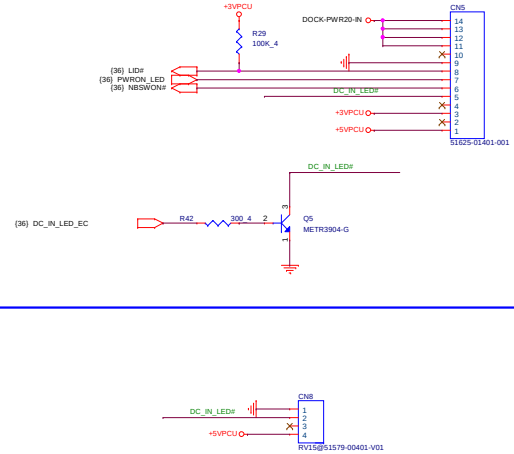
Prolink <DOK>



DP HPD SENSE



Power board w LED <UIF>



C3A

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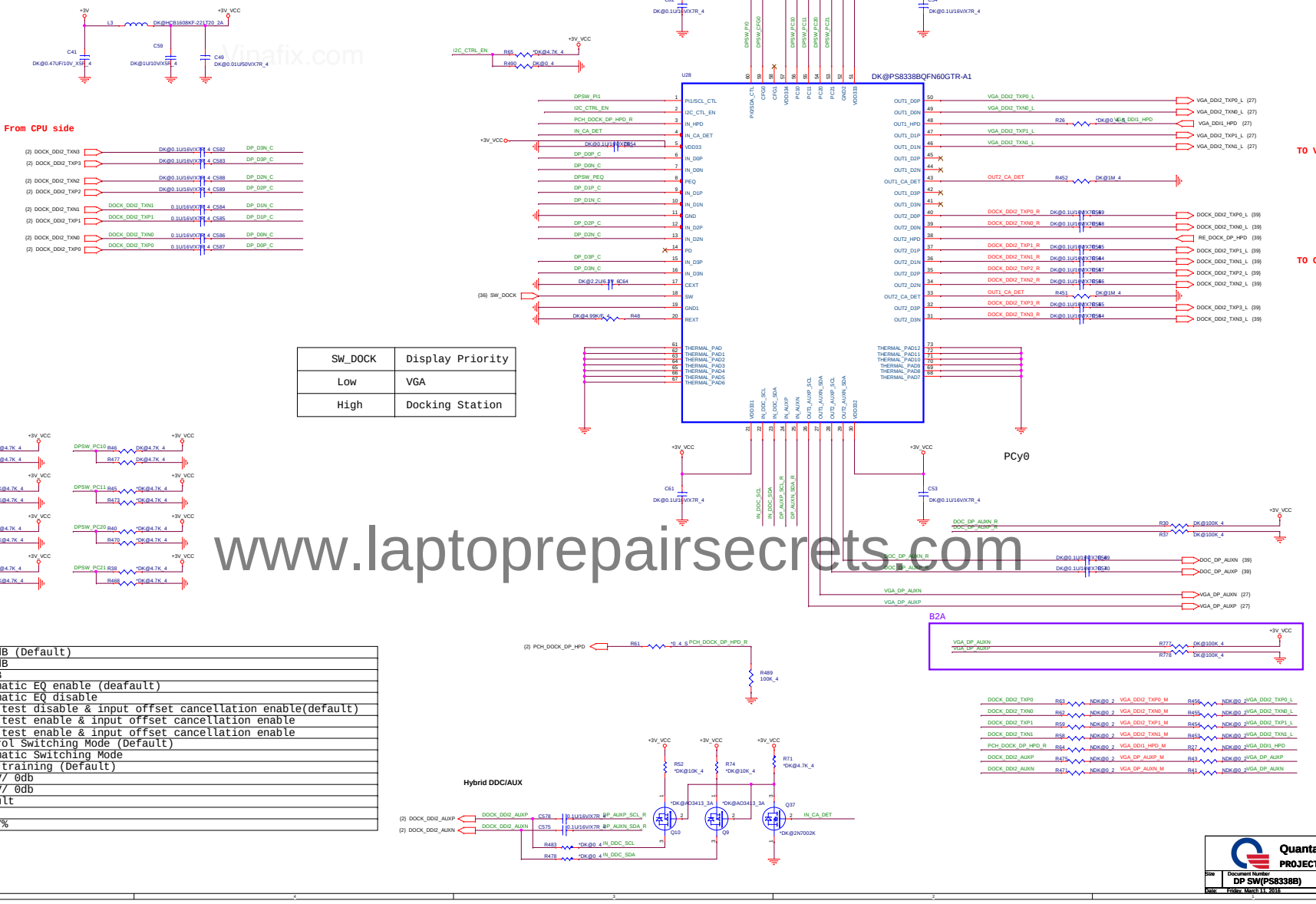
DP SWITCH **<DPP>**



SW_DOCK	Display Priority
Low	VGA
High	Docking Station

PEQ	L	11.5dB (Default)
	H	14.5dB
	M	8.5dB
PI0	L	Automatic EQ enable (deafault)
	H	Automatic EQ disable
PI1	L	Auto test disable & input offset cancellation enable(default)
	H	Auto test enable & input offset cancellation enable
	M	Auto test enable & input offset cancellation enable
CFG0	L	Control Switching Mode (Default)
	H	Automatic Switching Mode
PCy0 (AUX Interception)	L	Link training (Default)
	H	800mV/ 0db
	M	400mV/ 0db
PCy1 (Swing)	L	Default
	H	+20%
	M	-16.7%

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HOLE

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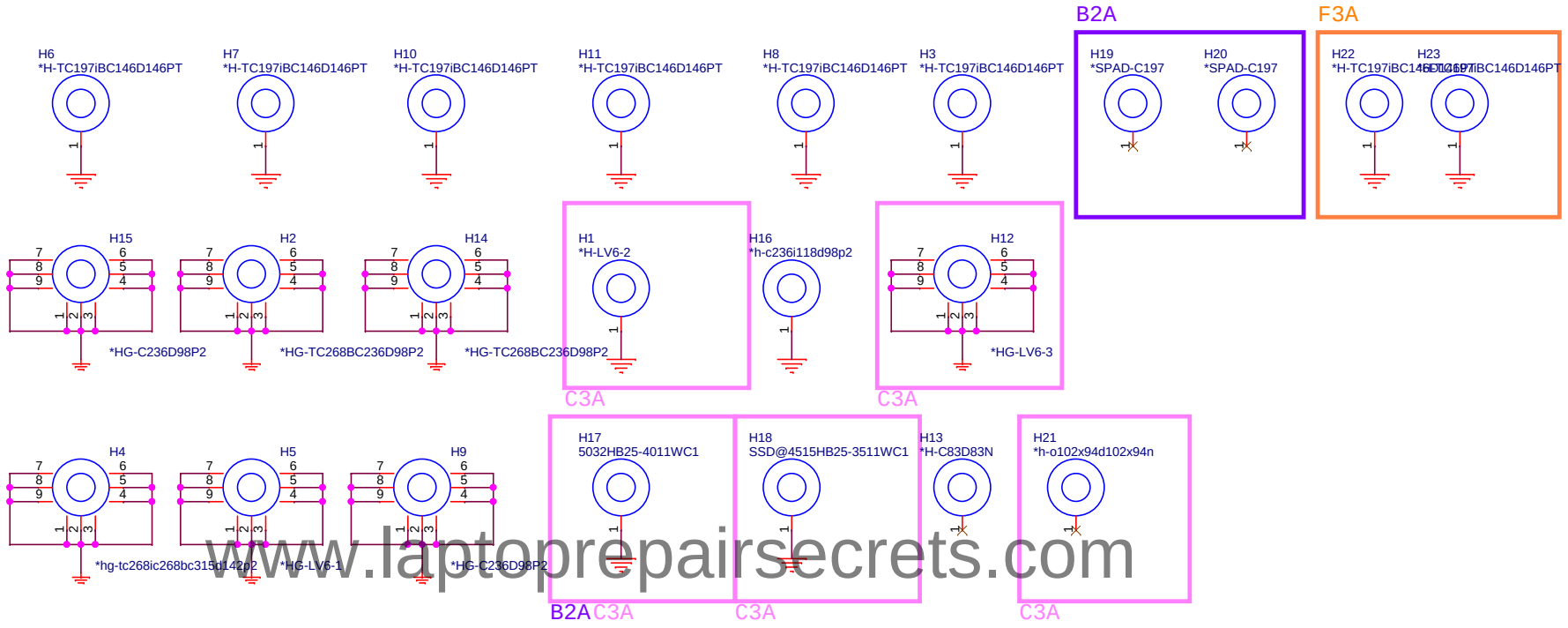

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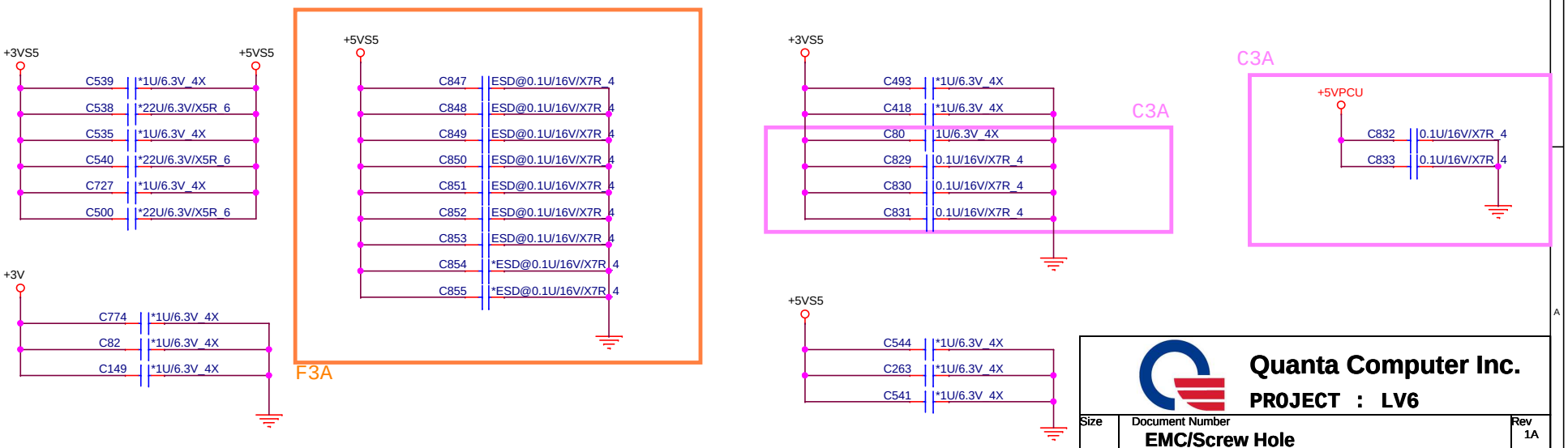
<EMC>



Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: EMC/Screw Hole	Rev: 1A
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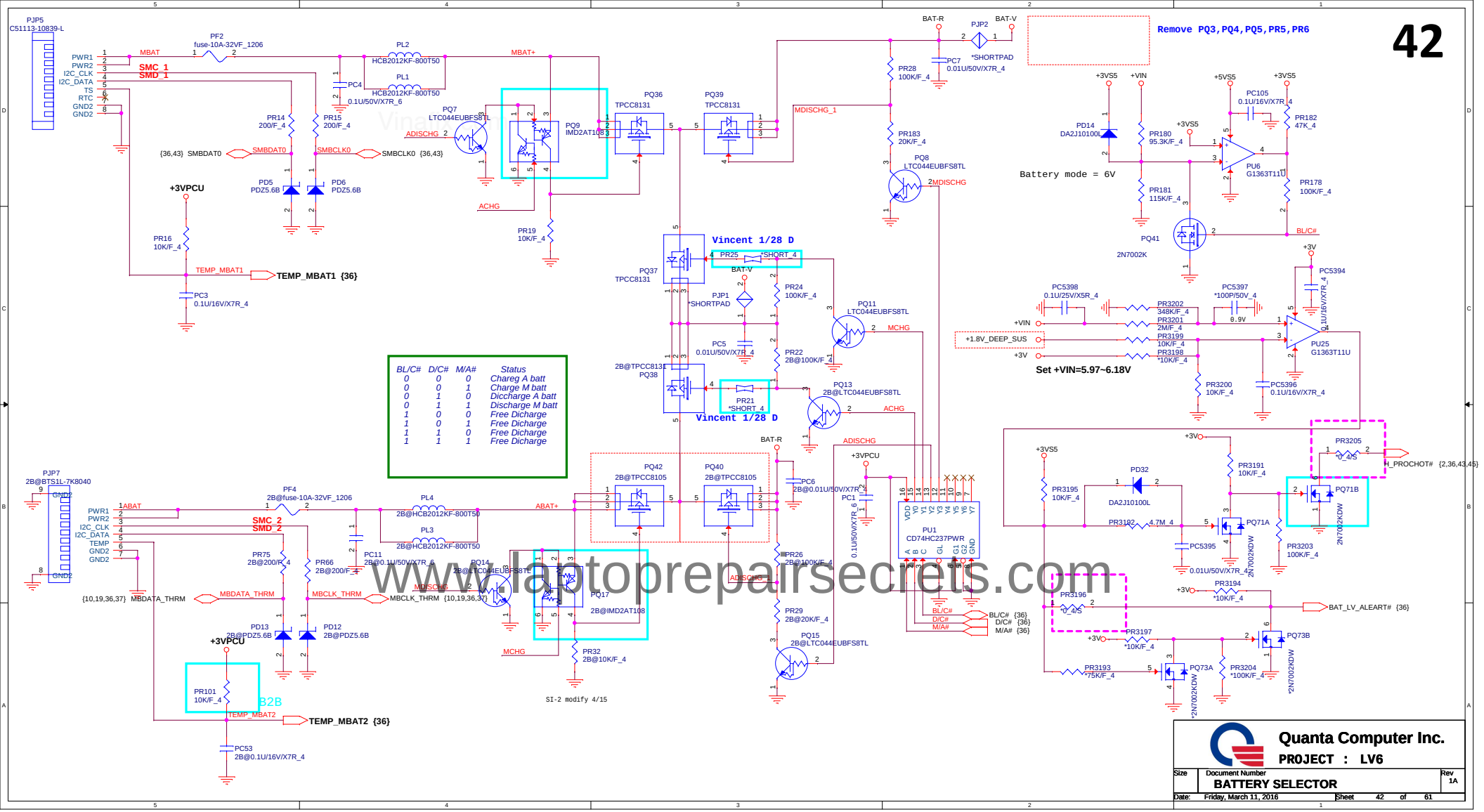

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Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number	Rev
	BATTERY SELECTOR	1A
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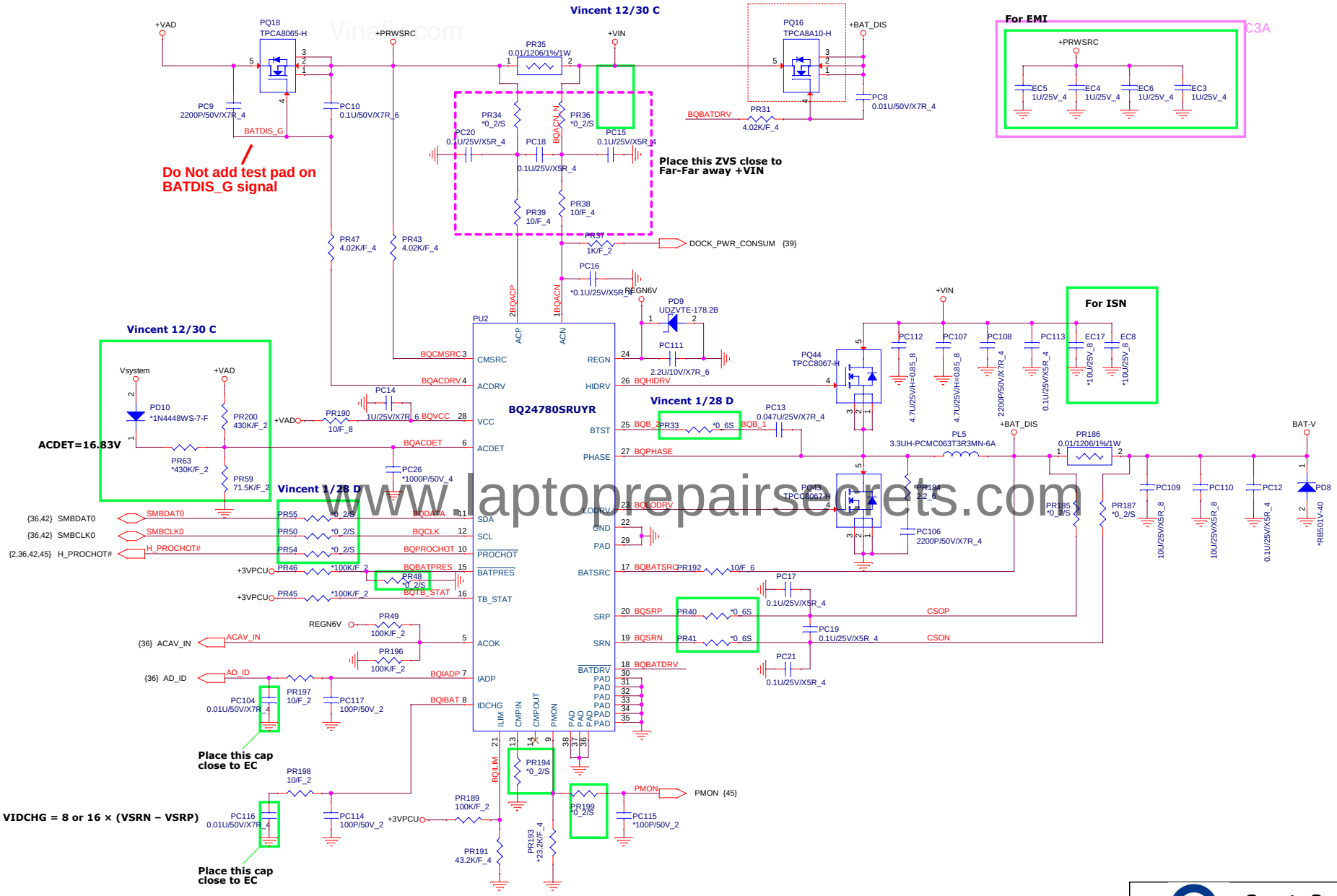

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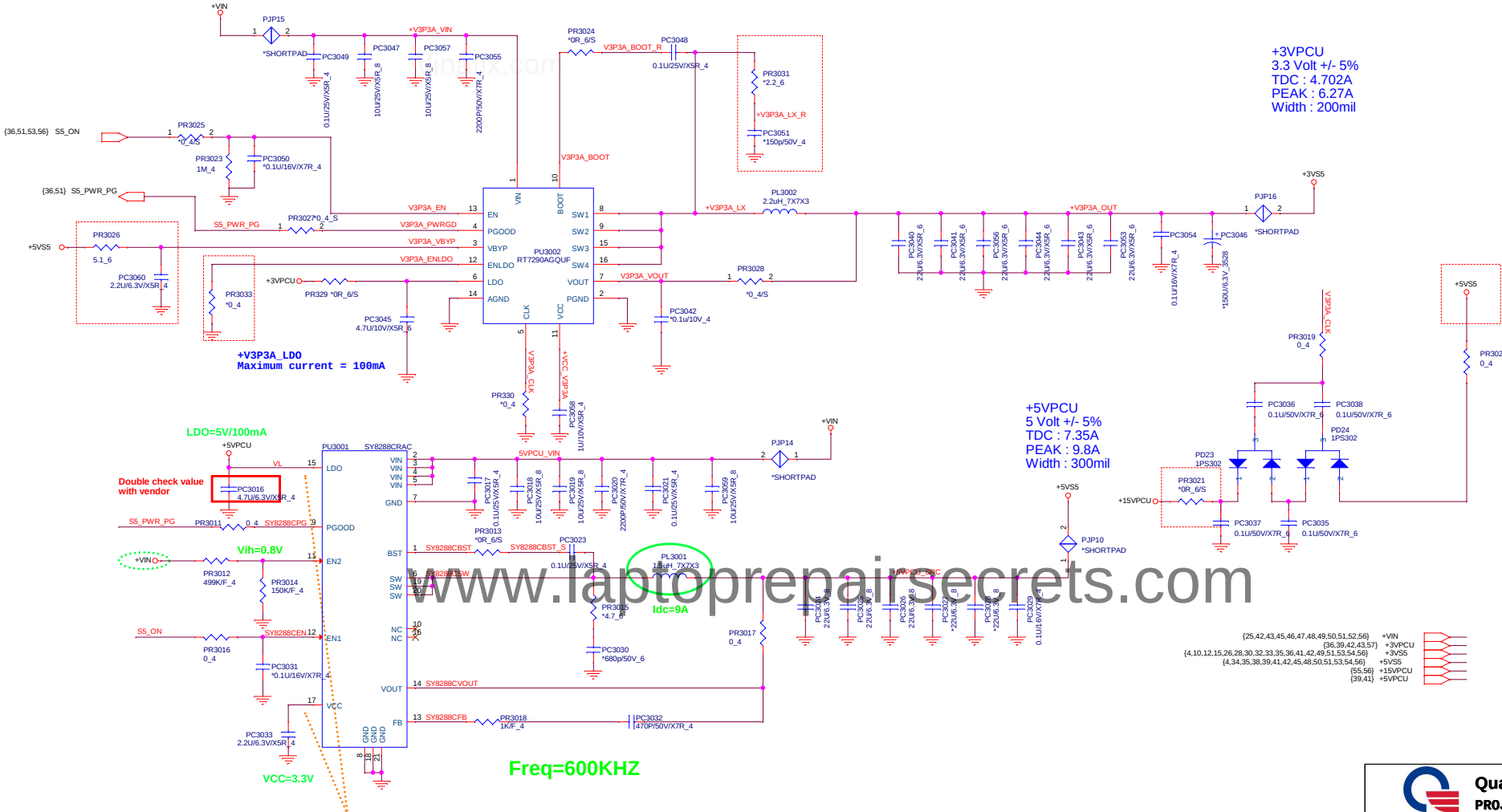

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Quanta Computer Inc.	
PROJECT : LV6	
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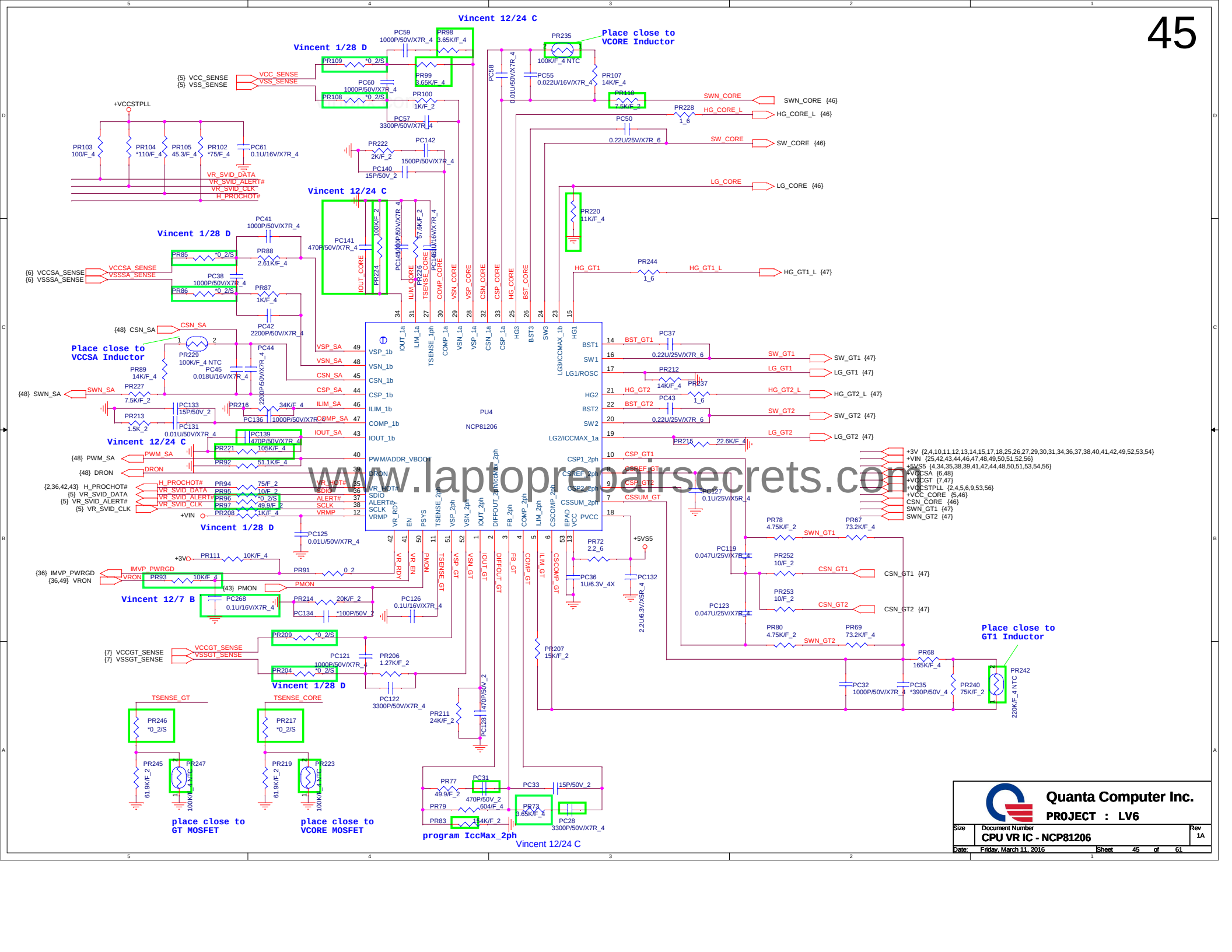
Vincent 12/24 C
Vincent 1/28 D
Place close to VCORE Inductor
Vincent 12/24 C
Vincent 1/28 D
Vincent 12/24 C
Place close to VCCSA Inductor
Vincent 1/28 D
Vincent 12/24 C
Vincent 12/7 B
Vincent 1/28 D
Place close to GT1 Inductor
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
Vincent 12/24 C
PU4
NCP81206
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Quanta Computer Inc.
PROJECT : LV6
CPU VR IC - NCP81206
Size
Document Number
Rev 1A
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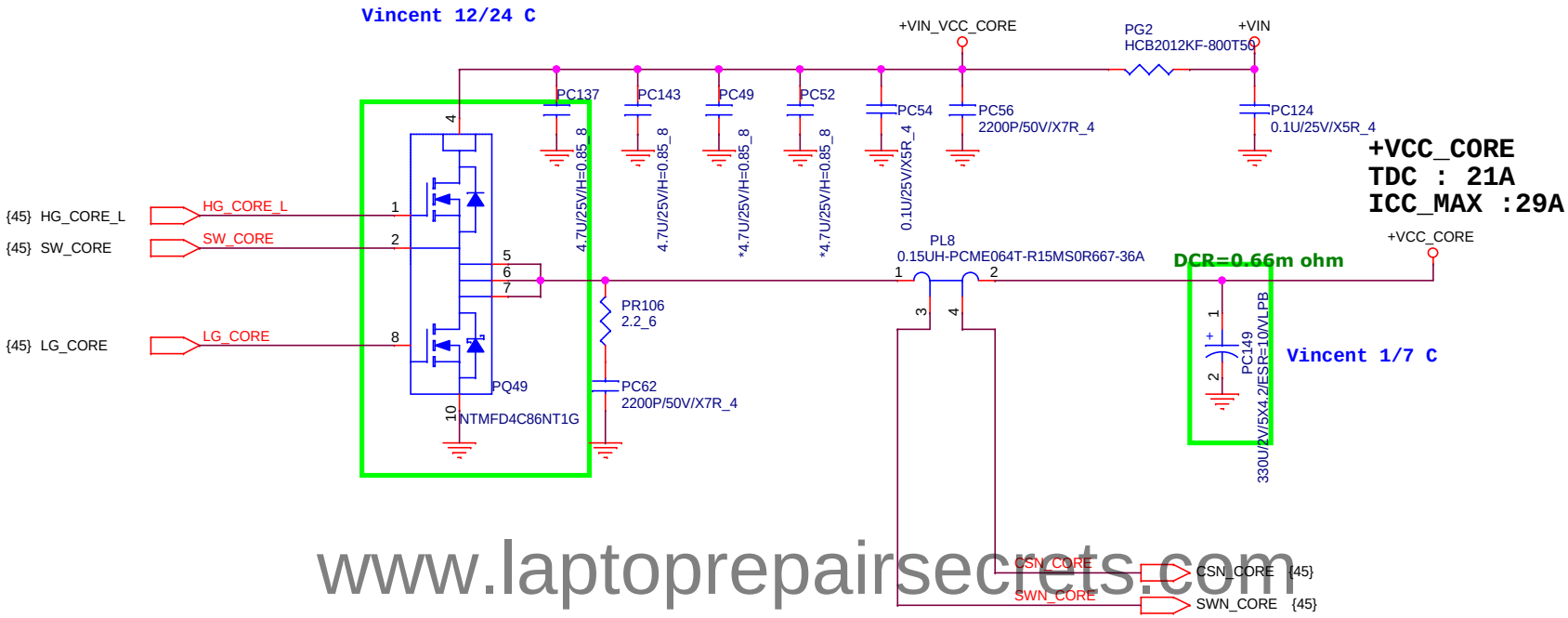
Vinafix.com



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Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: VCCORE	Rev: 1A
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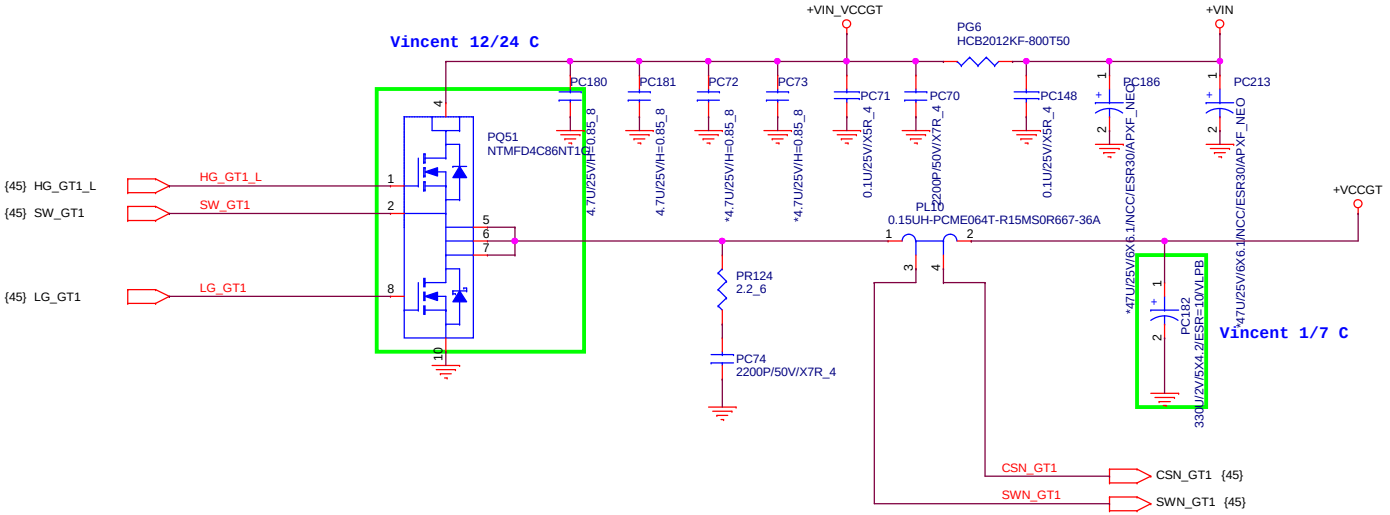
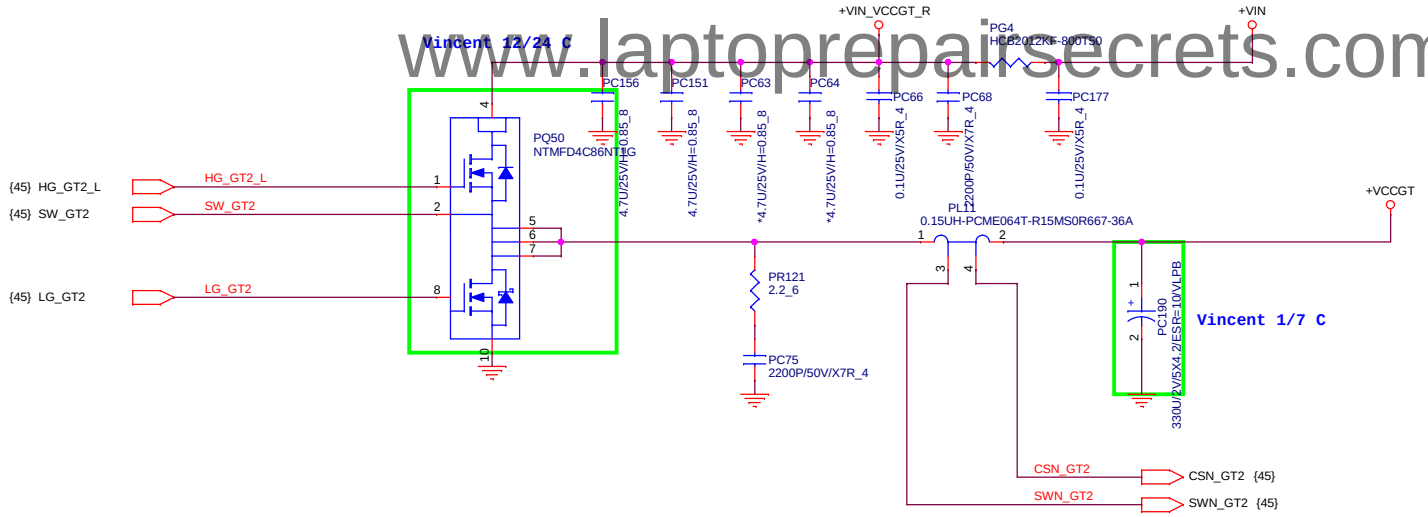
Vinafix.com





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+VCCGT
TDC :A
ICC_MAX :64A

Quanta Computer Inc.		
PROJECT : LV6		
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VCCSA

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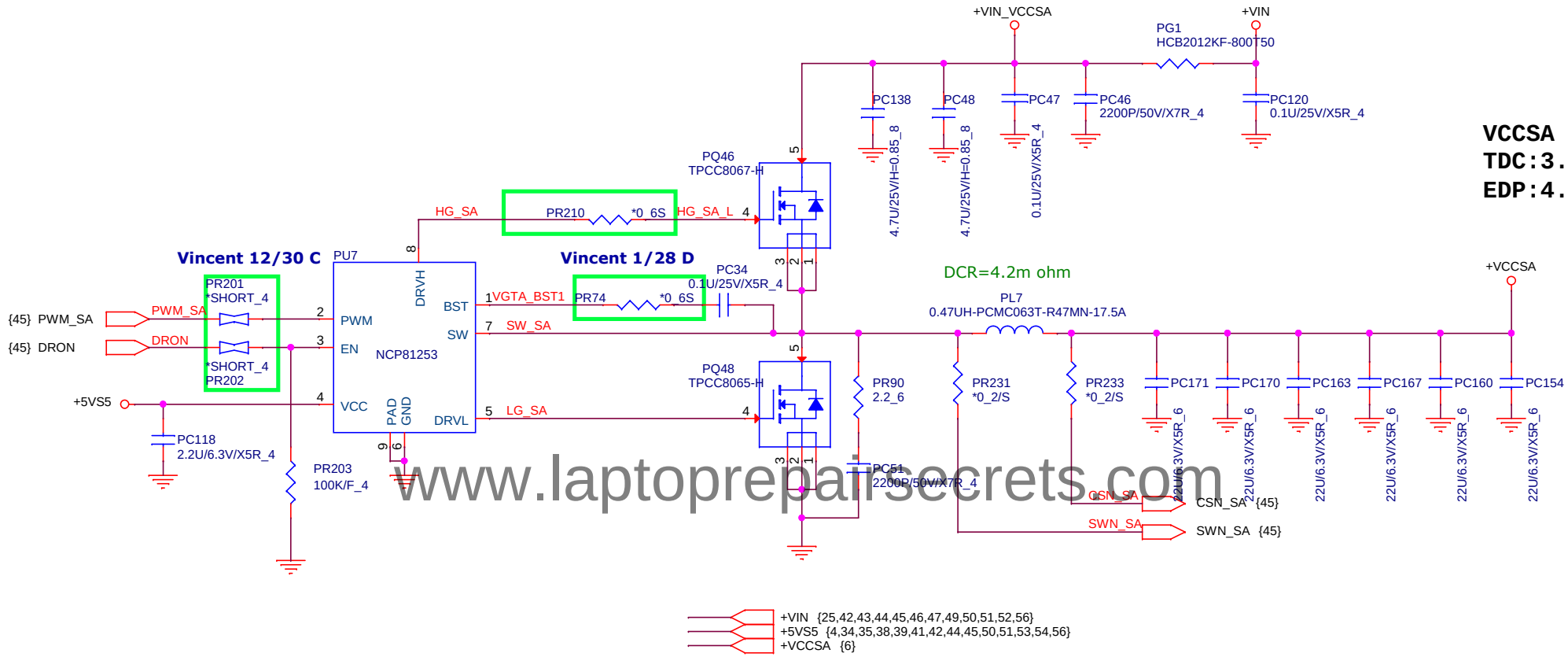

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Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: VCCSA - NCP81253	Rev: 1A
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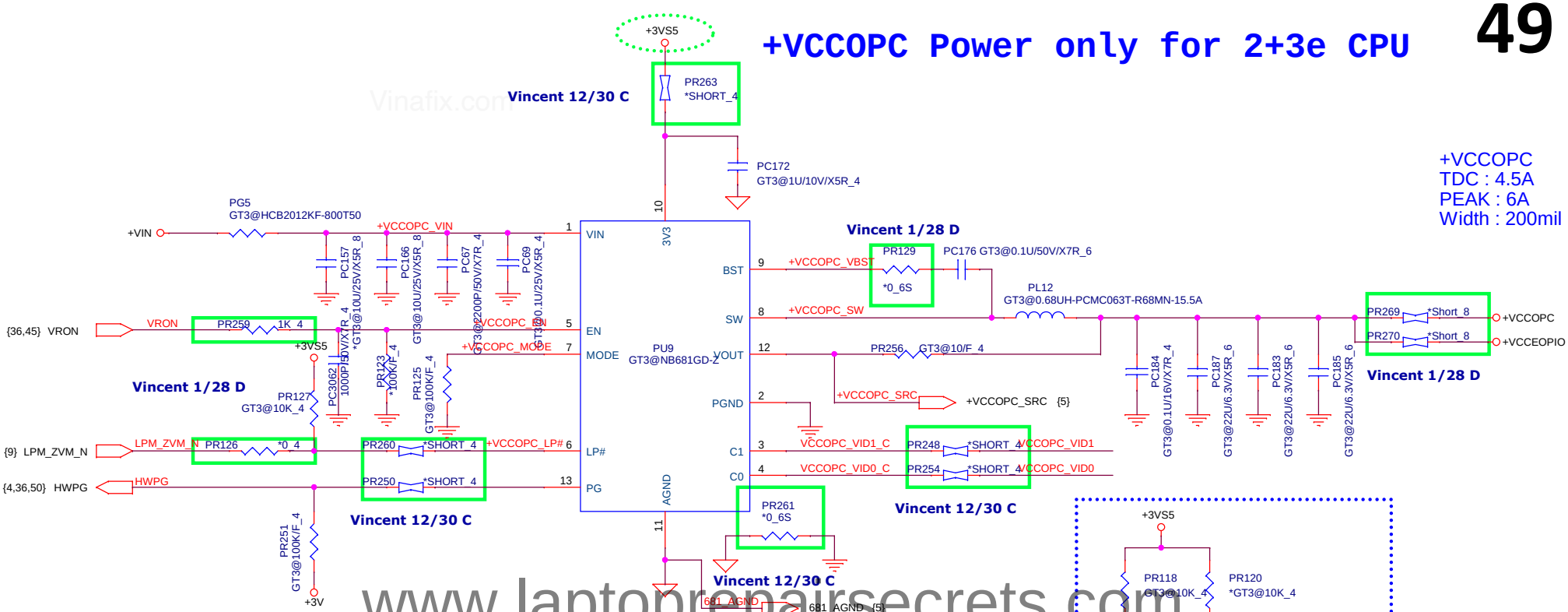
+VCCOPC Power only for 2+3e CPU



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Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM)
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

{5} +VCCOPC
{25,42,43,44,45,46,47,48,50,51,52,56} +VIN
{2,4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,52,53,54} +3V
{4,10,12,15,26,28,30,32,33,35,36,41,42,44,51,53,54,56} +3VS5

Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	+VCCOPC (NB681GD-Z)	1A
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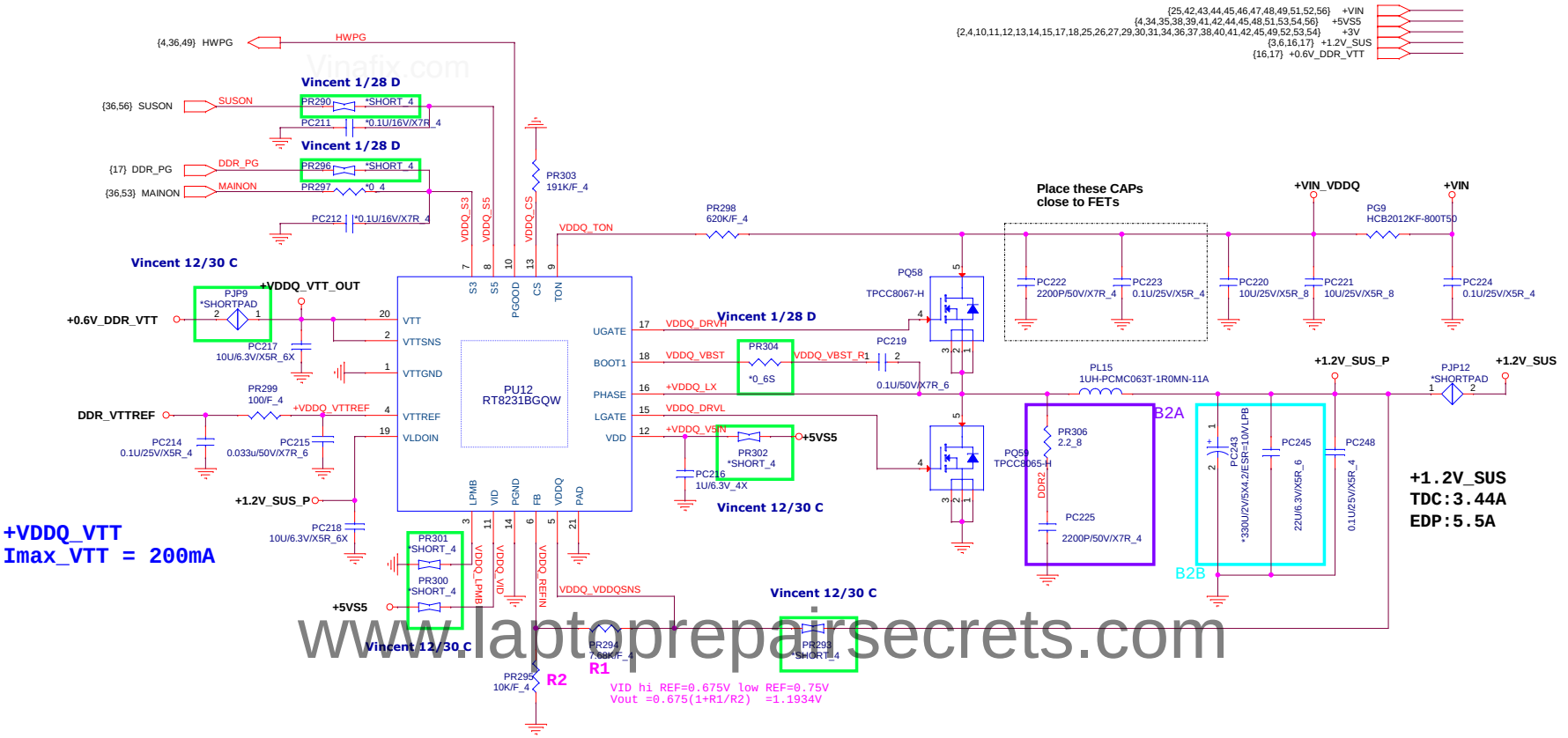
VR PAGE: +VDDQ

Fsw=500kHz



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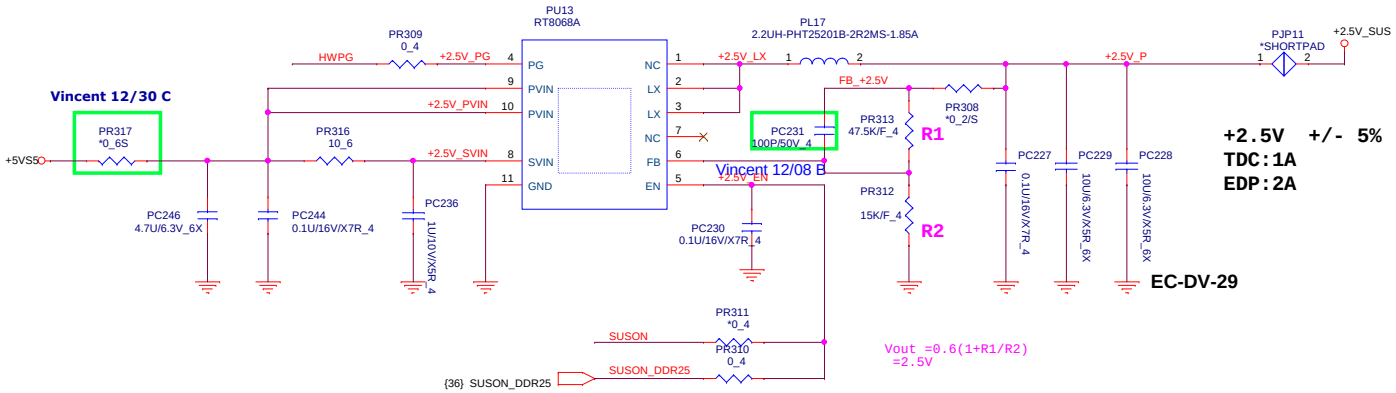

Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: VDDQ - TPS51716	Rev: 1A
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V1P0A (RT8237CZQW)

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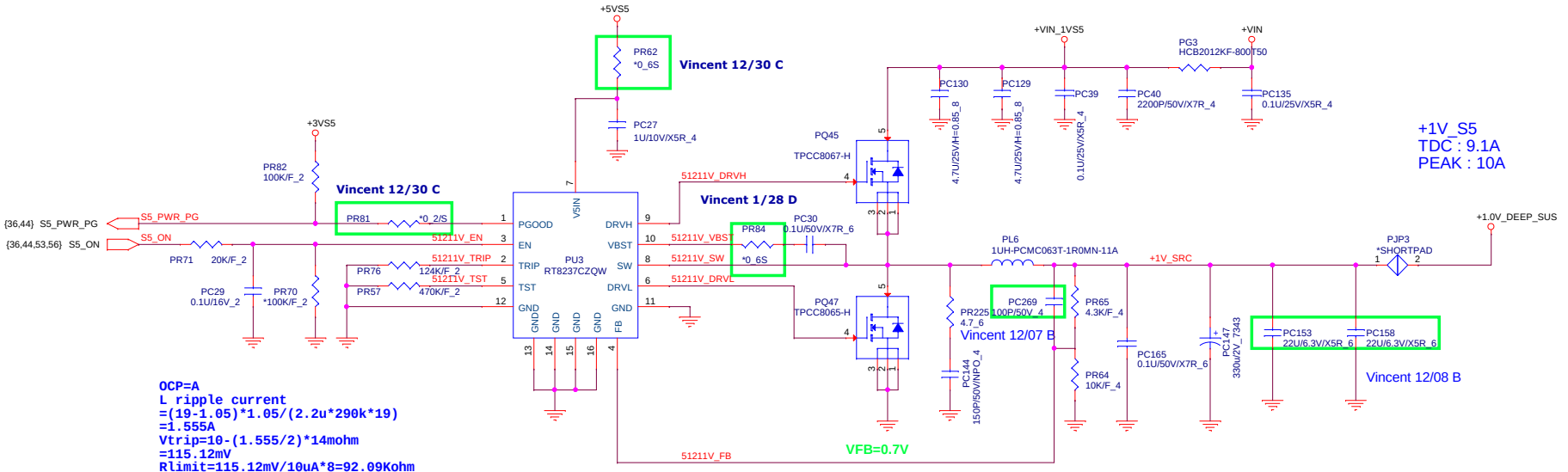

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Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: +1V_DS - RT8237CZQW	Rev: 1A
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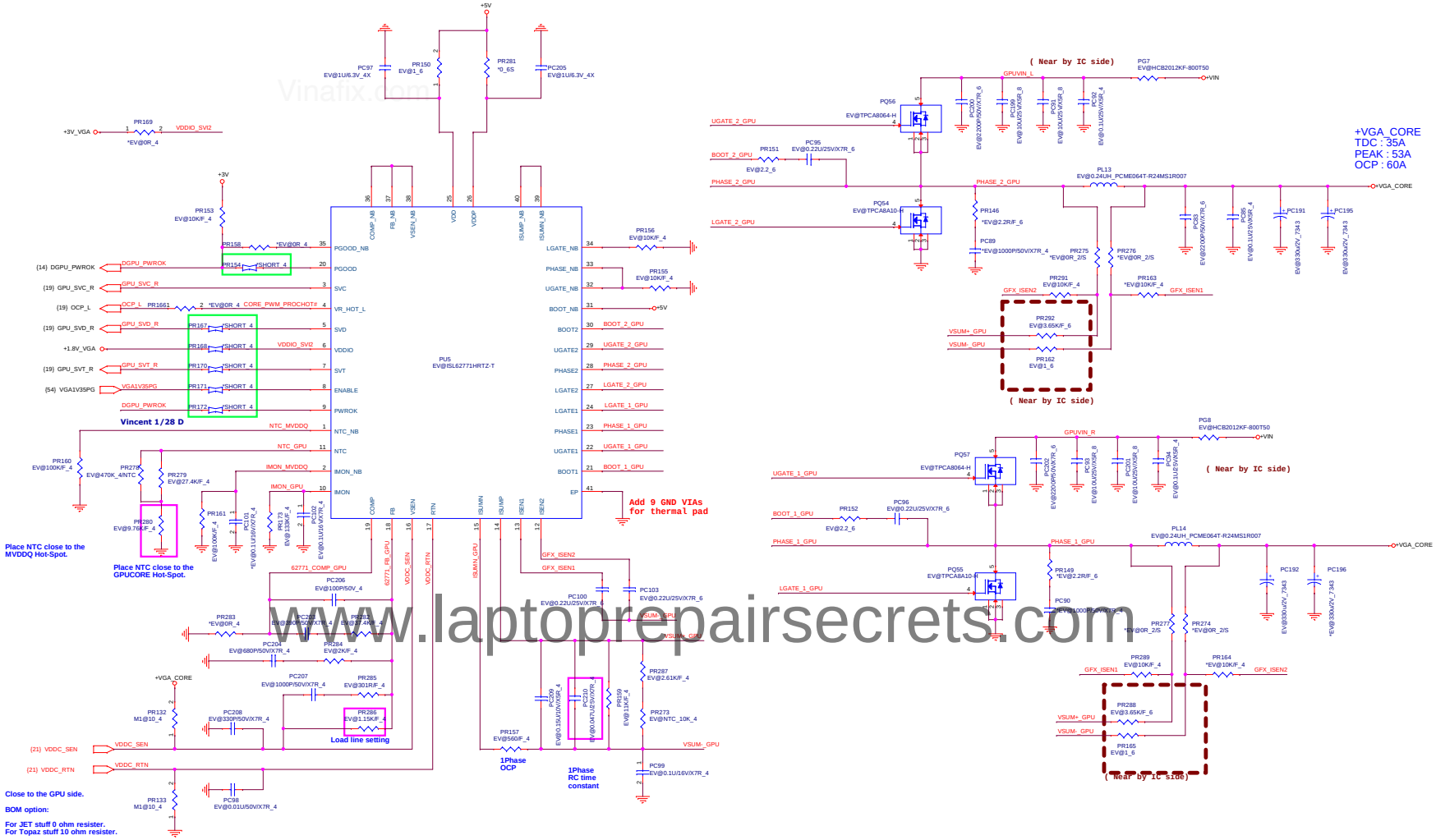
VGA-CORE



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Quanta Computer Inc.	
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Size	Document Number: GPU_CORE (ISL62771) — Rev: 1A
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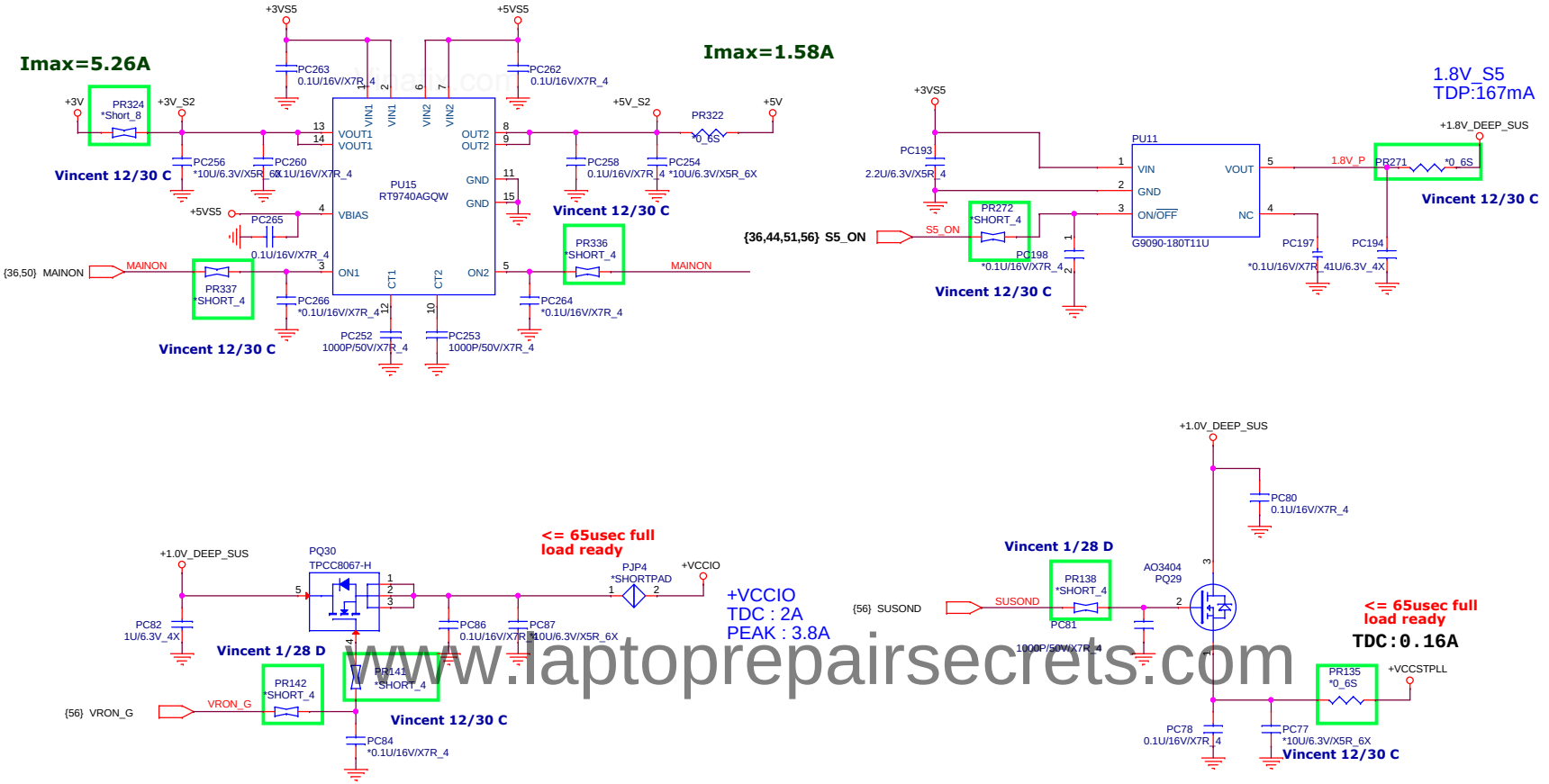

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Quanta Computer Inc.

PROJECT : LV6

Size	Document Number	Rev
	+1.0V/+3V/+5V SW	1A

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+1.8V_VGA(G9090-180T11U)
+1.35V_VGA(RT8068A)

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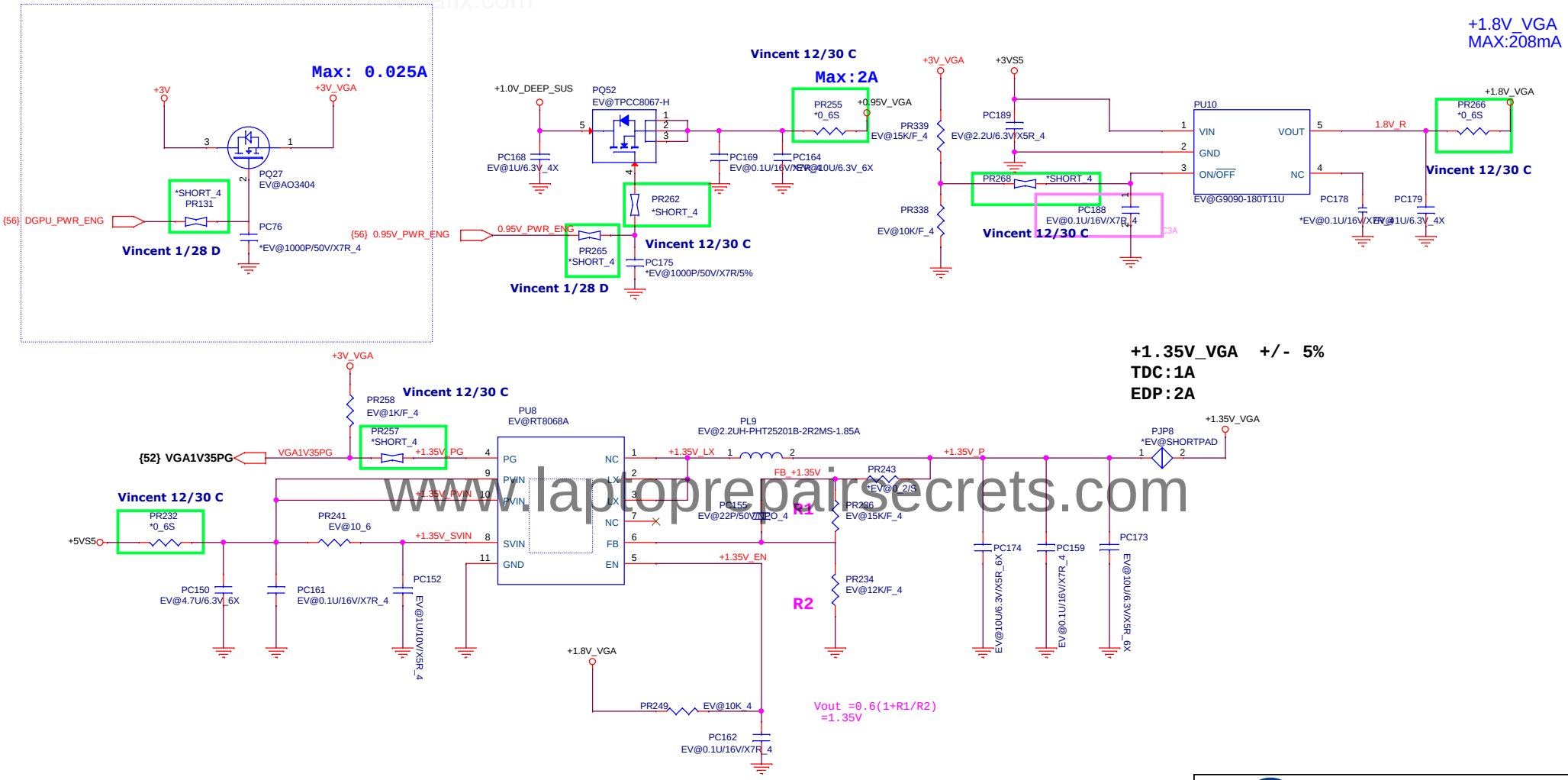

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Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: +1.8V/+1.35V/+3V_VGA	Rev: 1A
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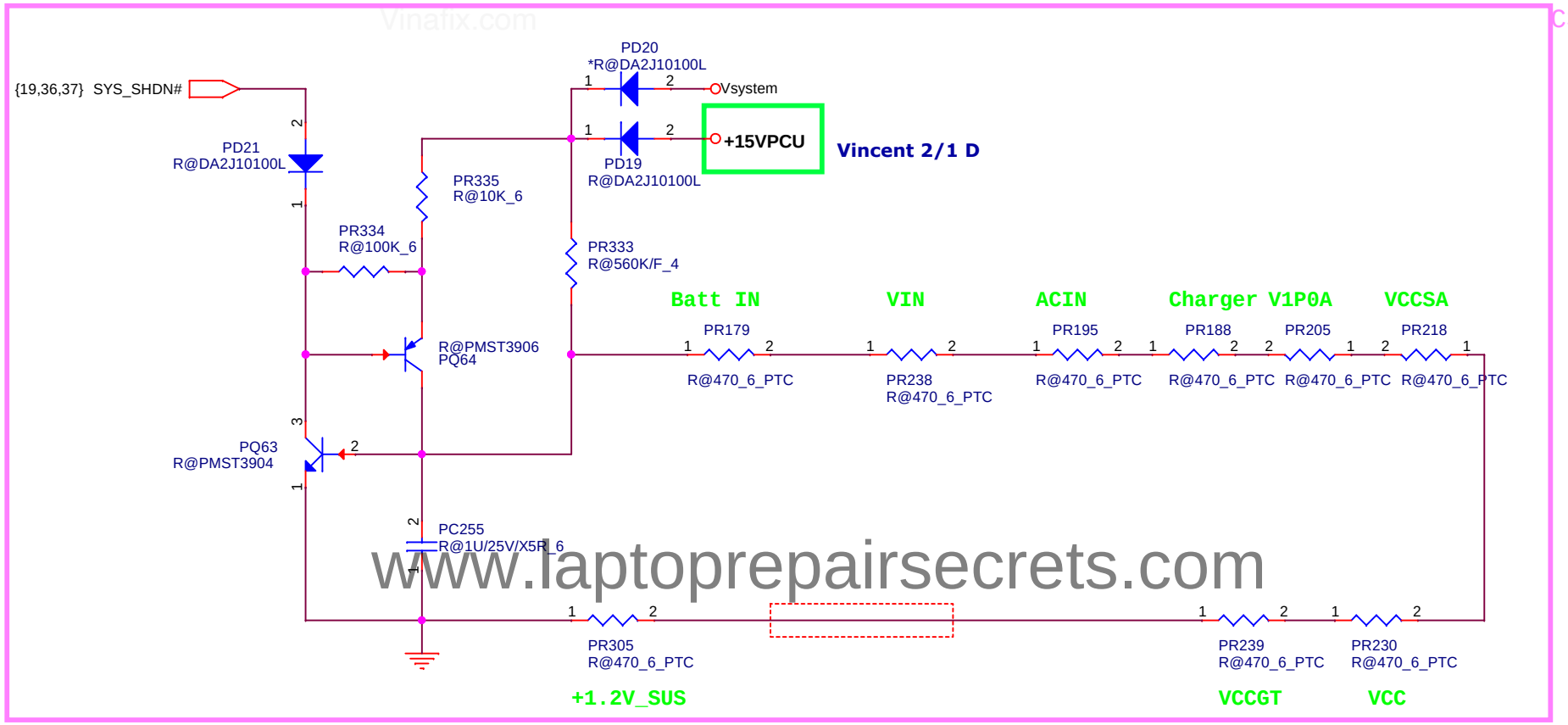
Vinafix.com



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Quanta Computer Inc.		
PROJECT : LV6		
Size	Document Number: PTC Circuit	Rev 1A
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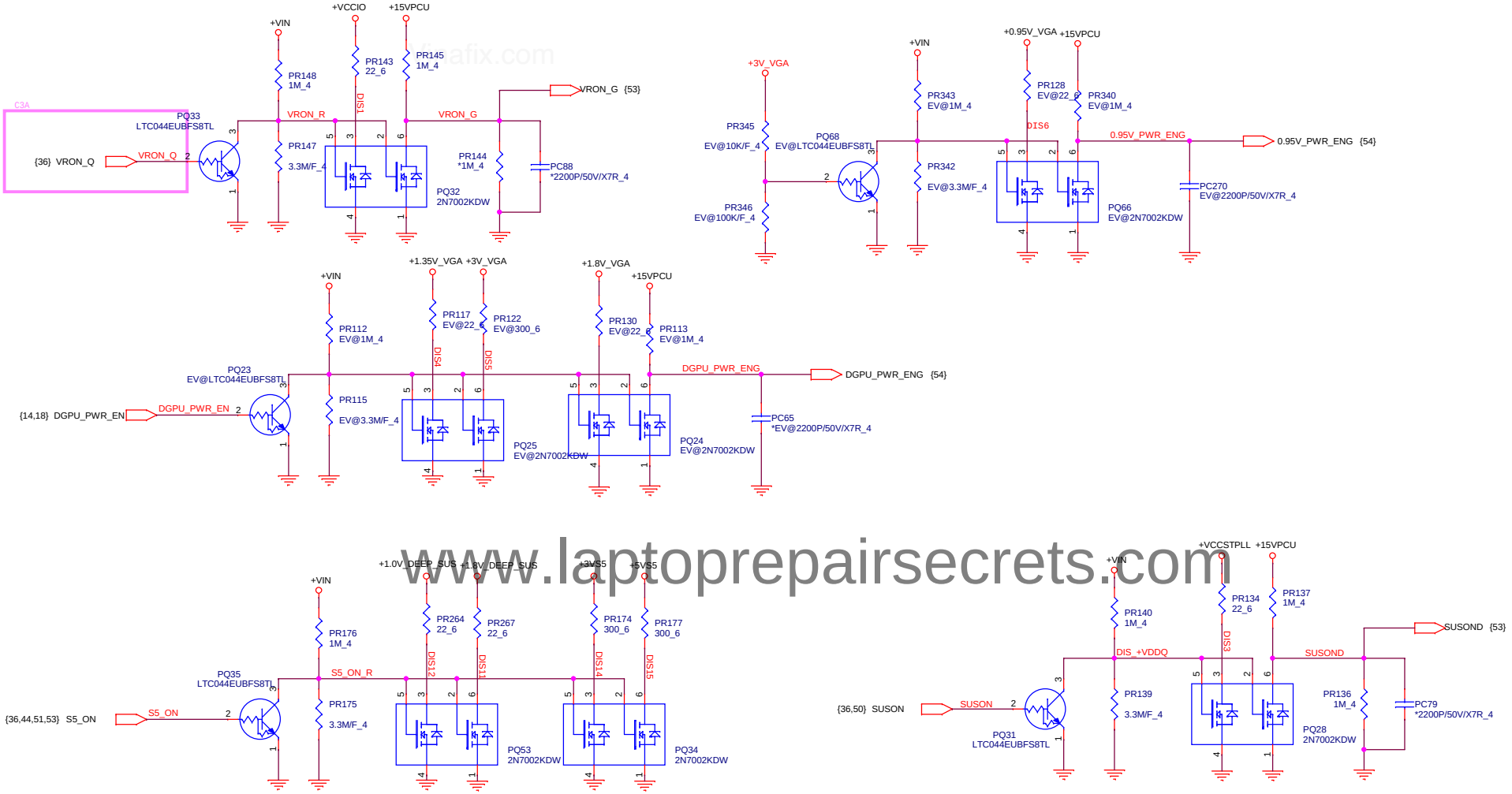
DISCHARGE



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Quanta Computer Inc.		
PROJECT : LV6		
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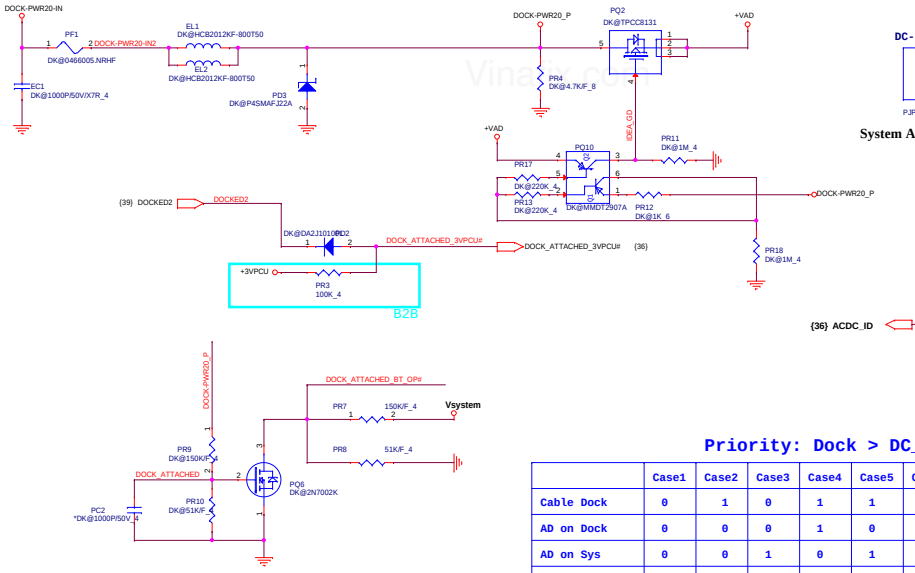
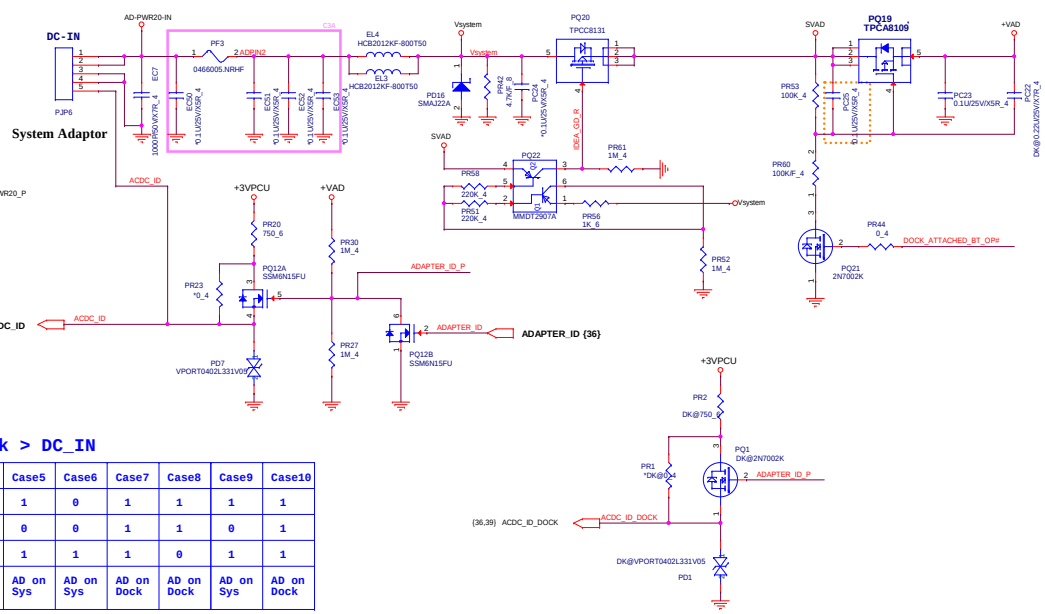
For Dock



For System



Priority: Dock > DC_IN

	Case1	Case2	Case3	Case4	Case5	Case6	Case7	Case8	Case9	Case10
Cable Dock	0	1	0	1	1	0	1	1	1	1
AD on Dock	0	0	0	1	0	0	1	1	0	1
AD on Sys	0	0	1	0	1	1	1	0	1	1
Power Source	Batt	Batt	AD on Sys	AD on Dock	AD on Sys	AD on Sys	AD on Dock	AD on Dock	AD on Sys	AD on Dock

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PROJECT : LV6
Size | Document Number: Power Source In Gate | Rev: 1A
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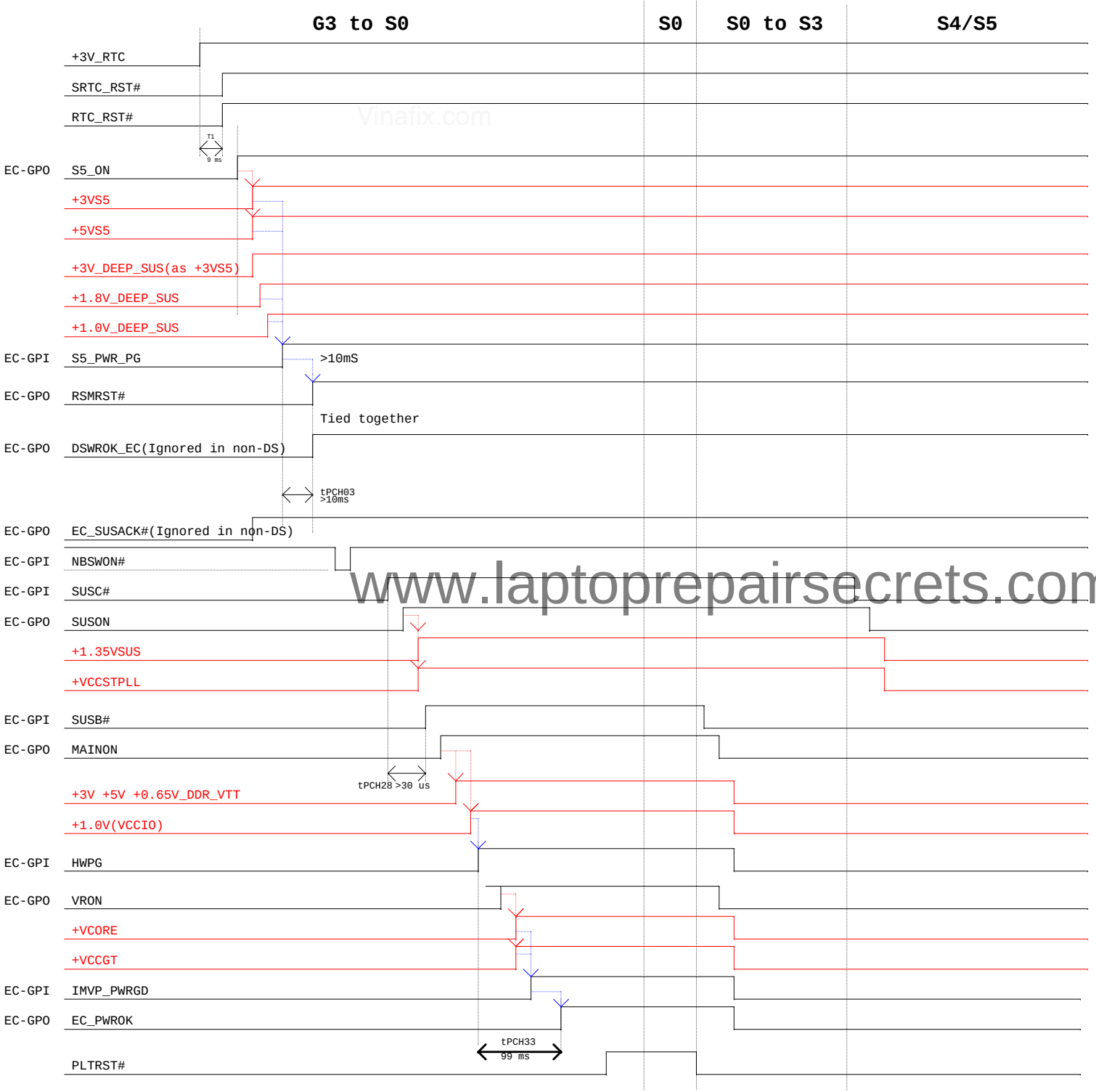

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Quanta Computer Inc.
PROJECT : LV6

Size	Document Number	Rev
	Power sequence2	1A

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	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2015 SDV-STAGE	B2A	2	12/7	R780	Reserve PU 10K for
		4	12/7	R763	Add PU Res 10K for LAN_WAKE#.
		4	12/7	R764	Add PU Res 10K for VRALERT#.
		5	12/7	C819	Add Cap 1U for VCCSTG_G20.
		14	12/7	R768, R767	Add Board ID for SKYLAKE/ KABYLAKE.
		26	12/7	R769、R770、R771、R772、R773、R774、R775、R776	Add ohm for HDMI test
		30	12/7	CN14	Modify LAN connect pin define for LED
		31	12/7	CN19	Remove GND of stand pin for HDD connect
		31	12/7	CN12	Modify ODD connect to match FFC pin define
	B2B (R310)	30	12/18	CN14	Modify LAN connect pin define for LED
		4, 36	12/18	D10、R779、R780	Reserve DNBSWON# PU to +3VS5 and short 0 ohm
		13, 30	12/25	C755、C763、C359、C360	RTC CAP tuning
		29	12/25	R21、R16、R3、R8	FOR EMI

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Size	Document Number	Rev
	EC list 1	1A

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2015

SIV-STAGE

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
C3A	4	1/8	R780	Reserve PU 10K for DNBSWON#
	4	1/8	U54、R781	Reserve PCH_SLP_S0# for power sequence
	12、13、39	1/8	C2、C3、C5、C6、C7、C8、C9、C10、C12、C13、C14、C16、C17、C18、C23、C549、C552、C553、C561、Q1、Q2、Q4、R1、R2、R4、R5、R17、R18、R19、R20、R445、R457、R462、TP29、U26、Y3、C700、C701	Remove DOCK LAN
	25、32、33、38	1/8	F2、F4、F7、F8	Change fuse to short pad
	30	1/8	CN14	Modify LED control signal
	34	1/8	C821、C822、C823、C824、R783、R784、R785、R786、C825、C826、C827、C828、R787、R788、R789、R790	Reserve EMI request
	36	1/8	R779	Reserve 0 ohm to jump diode for DNBSWON#
	38	1/8	R323、R329	Mount keyboard RES
	39	1/8	CN3	Change connect from 40 pin to 30 pin that remove DOCK LAN
	14	1/8		No memory down config
	41	1/8	C829、C830、C831、C832、C833	Add CAP for EMI request
	43	1/8	EC3、EC4、EC5、EC6	Add CAP for EMI request

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	EC list 2	1A

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2015

SIT-STAGE

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION

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	EC list 3	1A

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